MINDSPEED®

Product Brief

# PC205 Multi-Core DSP for Wireless Infrastructure

## PC205 Features

- picoArray Scalable Architecture
- ARM®926EJ-S Processor
  - 64KB I + 64KB D cache
  - 128KB Tightly Coupled Memory (TCM)
  - 128KB on-chip SRAM
  - RS-232/JTAG for debug
- Dual Correlation Block
- FFT Accelerator of 4x FFT/IFFT
  - OFDM
  - AAS/MIMO systems
- Integrated Cryptographic Engine
  - AES, DES, 3DES
- FEC Accelerator
  - CTC error correction
  - Reed-Solomon Block FEC
  - Viterbi
- 10/100 Ethernet MAC and MII
  - Reverse MII mode
- DDR2 SDRAM Interface
  - 16/32-bit
  - 200MHz clock
  - 256Mbit to 2Gbit
- Three External Interfaces (ADI)
  - Two independent 16-bit I/O channels each
  - Multiple RF Interfaces
  - Multi-PC203 Interconnect
- General Purpose I/O - 32 pins
  - SIM Interface
  - Sigma Delta DAC
  - SPI/I$^2$C
- Software update for “future-proof” systems
- Industrial Temperature Range
- 672 PBGA Package (27x27)

## Description

The picoChip PC205 is a highly integrated and high performance baseband processor for broadband wireless access points. The PC205 offers multi-device interconnect and higher speed baseband accelerators compared to the PC202 for improved baseband performance in high demand access points or small basestations.

The PC205 consists of a flexible software defined modem, ARM®926EJ-S processor, cryptographic engine, high-speed co-processors, and peripherals to support popular wireless communication protocols such as WiMAX and WCDMA. All Physical layer (PHY), lower MAC, upper MAC, and cryptographic features are integrated enabling a greatly reduced BOM.

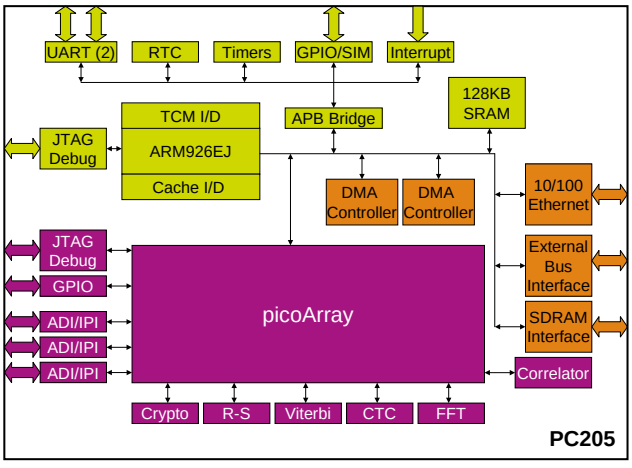
Associated software libraries are available to support both WiMAX and HSDPA systems, greatly reducing development effort and time to market. The system supports upgrades (future-proof) to support interoperability, changes to the standard, or manufacturer-specific features.

A scalable architecture allows connection of the PC205 to one or more PC203’s for increased processing bandwidth in compute intensive applications like MIMO, smart antennas, and beam forming. Standardizing on the PC205 allows developers to build small basestations or high bandwidth access products in a manner that preserves the ability to build a full range of basestations from a single technology base.

The PC205 is available in two versions. The PC205 has 248 processors in the picoArray. The PC205-10 has an additional row of picoArray processors. The PC205-10 has 273 picoArray processors in total.

## PC205 Applications

- WiMAX 802.16d, 802.16e, WiBRO
  - Femtocells
  - Basestations
  - Mesh nodes
  - WiFi access point backhaul
- HSDPA/HSUPA Picocells
- WCDMA-TDD/TD-SCMA
- Advanced Wireless
  - AMC
  - MIMO




**PC205 Block Diagram**



Preliminary Information.

# PicoArray Sub-System

The picoArray is a software defined signal processor responsible for executing the PHY and lower MAC software. (Upper MAC functions are performed in the ARM® processor block.) The picoArray's flexibility allows software upgrades to be applied as necessary in-line with product releases, localizations, standardization updates, bug fixes, and performance enhancements.

The flexibility and scalability of the picoChip architecture allows developers to create a range of products from small basestation solutions (femtocell or picocells) up to full-sized multi-sector cells with advanced functions such as MIMO and higher bandwidths and data rates. All of this is achieved using the same base architecture.

**Multicore DSP Array (picoArray)**

The picoArray consists an array of LIW DSPs (AEs) capable of up to 6 operations per cycle. Each AE has dedicated instruction memory and data memory. Each AE also has access to shared on-chip SRAM and off-chip DRAM. Dedicated instruction and data memory for each processor means very little contention for shared memory resources. There are three different types of AEs in the PC203. The table on the right lists the number and type of each AE along with its total memory sizes.

| | PC205 | | PC205-10 | |
|---|---|---|---|---|
| AE Type | Number of AEs | Memory (Bytes) | Number of AEs | Memory (Bytes) |
| | | | | |
| STAN | 196 | 150,528 | 216 | 165,888 |
| MEM | 50 | 435,200 | 55 | 478,720 |
| CTRL | 2 | 131,072 | 2 | 131,072 |
| Total | 248 | 716,800 | 273 | 775,680 |

Flexible interconnect provides point-to-point and point-to-multipoint connections between any two AEs with dedicated bandwidth.

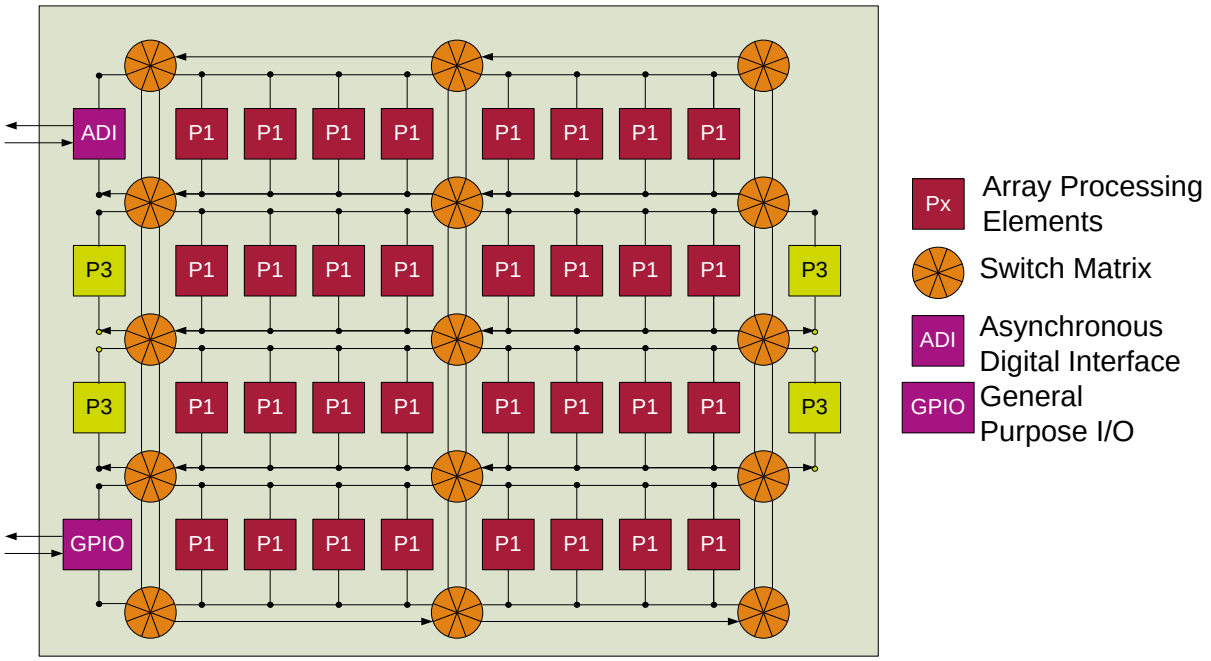



**Figure 1 picoArray of DSP Processors and Interconnect**

**Convolutional Turbo Code (CTC) Block**

The Convolutional Turbo Code (CTC) is mandatory in TTA WiBRO and optionally required in the WiMAX SOFDMA air interface of IEEE802.16e. The CTC block is capable of supporting rate 1/3 turbo encoding as required in HSDPA systems. The CTC algorithm allows much enhanced bit error rates in a given data channel compared to CC and R-S coding. Rates from 18 to 60 Mbps are supported.

**FFT/IFFT**

FFT/IFFT hardware accelerator is designed to optimise the performance of OFDM/OFDMA based systems. PC205 supports up to 4 parallel complex FFTs, to accelerate multiple receive chain processing in OFDM systems, such as that found in AAS and MIMO based systems.

The FFT engine can support complex FFT sizes of 128, 256, 512 and 1024 points; extendable to 2048 points in software. Features of the FFT block include on-the-fly FFT/IFFT, 16-bit input and output with scaling, bit reversal capability and a self-flushing mechanism.

| | PC205 | | PC205-10 | |
|---|---|---|---|---|
| **Feature** | **Perf.** | **Units** | **Perf.** | **Units** |
| picoArray | 31 | GMAC/s | 35 | GMAC/s |
| | 230 | GIP/s | 262 | GIP/s |
| | 8 | GMUL/s | 9 | GMUL/s |
| FFT (aggregate) | 320 | MS/s | 320 | MS/s |
| Crypto Engine | 40 | Mb/s | 40 | Mb/s |
| Turbo Code (8 iter.) | 18 | Mb/s | 18 | Mb/s |
| Viterbi | 40 | Mb/s | 40 | Mb/s |
| R-S | 40 | Mb/s | 40 | Mb/s |
| Correlator | 40 | Mb/s | 40 | Mb/s |
| ADI | 3x160 | MS/s | 3x160 | MS/s |
| ARM | 280 | MHz | 280 | MHz |

**Viterbi**

Viterbi hardware accelerator block is used to accelerate the Viterbi decoding process in wireless systems. The Viterbi block is optimised for WiMAX and HSDPA systems. It is configurable for constraint lengths of 2 to 9, and rates of 1/2, 1/3, 1/4, 1/5, 1/6, 1/7 or 1/8. Multiple puncturing rates are also supported. Block sizes are from 16 to 1024.

Supported standards include 802.16d, 802.16e, UMTS (TDD, FDD, HSDPA, HSUPA), CDMA2000, TD-SCDMA, 802.11a, b, g, GSM, GPRS, EDGE, and EGPRS.

**Reed-Solomon (R-S)**

The PC205 incorporates a Reed-Solomon accelerator block (up to 40Mbps) for use in R-S block decoding requirements.

**Cryptographic Engine**

On-chip support of the IEEE802.16 specified cryptographic suite is provided. The PC205 incorporates the support of AES, DES & 3DES algorithms as required by the MAC security sub-layer.

## ARM® Sub-System

The ARM® sub-system is based around the ARM®926EJ-S core from ARM® Ltd. This powerful 32-bit RISC processor is highly optimised for low power, high performance, computing for the MAC layer. Being an industry standard core, the ARM® is supported by various openly available tool chains and debuggers. JTAG ports support a simple and familiar development environment.

**ARM® Memory Architecture**

The memory architecture supports a full range of memory types, allowing flexible memory map allocation depending upon the particular application requirements. The cache and tightly coupled memory deliver maximum processor performance. The memory types are summarised as follows

- On-chip memory for maximum performance
  - 64KB instruction, 64KB data cache, 32 bits wide
  - 64KB instruction, 64KB data TCM (Tightly Coupled Memory), 32 bits wide single state access
  - 128MB SRAM, 32 bits wide, two state access
- External memory
  - DDR2-SDRAM via dedicated interface
  - NOR Flash for system boot and parameter storage

**ARM® Peripherals**

PC205 integrates a number of peripheral blocks allowing both a reduction in total system BOM cost, as well as providing flexible interfaces to application specific sub-systems. The ARM® peripherals are logically mapped into the ARM® memory map, and are conveniently configurable by way of dedicated registers per block. The principle ARM® peripheral blocs are summarised as follows:

- General purpose timer block e.g. for operating system tick

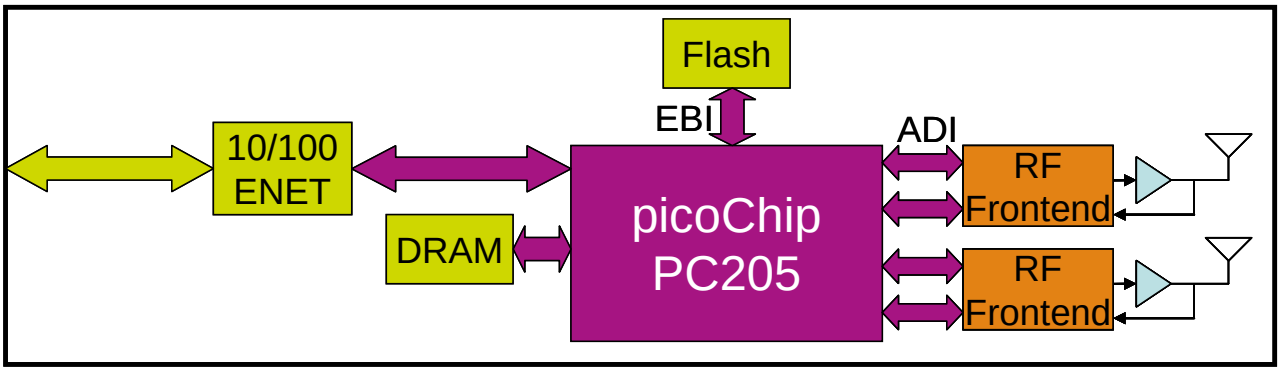
- Watchdog Timer
- Dual UART RS-232 interface for real-time tracing of MAC software
- 10/100 Ethernet MAC
  - Reverse MII interface allowing direct connection to MII interfaces of router/WiFi chipsets
  - Built-in DMA controller
- GPIO-SPI, I2C, SIM Card Interface
- Vectored Interrupt Controller

## Interfaces

- External Bus Interface (EBI) allowing connection to boot Flash memory or other memory interfaces or peripherals.
- Three shared Inter-picoArray Interfaces (IPI) allow high-speed interconnect to PC203's or picoChip's PC102 for more signal processing performance. This enables a scalable PHY architecture to support high performance signal processing such as advanced antenna algorithms required in demanding base-station applications.
- Three shared Asynchronous Digital Interfaces (ADI) for flexible baseband interfacing to data-converters (up to 2 antennas receive and transmit per ADI port). Each port consists of two 16-bit interfaces with a 160 MSps throughput and flexible handshake logic.
- DDR2-SDRAM memory interface supports different sizes and bus widths to create most economical memory solution.
- General Purpose I/O of 32 pins is programmable to support a number of different requirements such as SIM card for authentication, sigma-delta DAC for AGC, SPI, or $I^2C$
- JTAG test and debug allowing connection to picoICE debugger.

## Typical PC205 System

The PC205 is ideal for WiMAX femtocell applications where the internal ARM® processor can be used to implement the MAC functions. The increased picoArray and coprocessor performance allows for extended capacity and bandwidth over the PC203.




**PC205 System**

For applications that use WiMAX as in-home basestations, the increased bandwidth in the PC205 can support full WiMAX requirements while keeping the BOM small with the integrated ARM® processor. The integrated ARM® in each case may be used to implement the MAC functions for each network as well as protocol translation between the two networks.

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