ADSP-BF533 EZ-KIT Lite®
Evaluation System Manual

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Analog Devices, Inc.
One Technology Way
Norwood, Mass. 02062-9106

ANALOG DEVICES

Copyright Information

Printed in the USA.

Limited Warranty

The EZ-KIT Lite evaluation system is warranted against defects in materials and workmanship for a period of one year from the date of purchase from Analog Devices or from an authorized dealer.

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Regulatory Compliance

The ADSP-BF533 EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The ADSP-BF533 EZ-KIT Lite evaluation system had been appended to Analog Devices Development Tools Technical Construction File referenced "DSPTOOLS1" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

CONTENTS

PREFACE

EZ-KIT LITE HARDWARE REFERENCE

PREFACE

Thank you for purchasing the ADSP-BF533 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for Blackfin® processors.

The Blackfin processors are embedded processors that support a Media Instruction Set Computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics towards delivering signal processing performance in a microprocessor-like environment.

The evaluation board is designed to be used in conjunction with the VisualDSP++® development environment to test the capabilities of the ADSP-BF533 Blackfin processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C and ADSP-BF533 assembly
- Load, run, step, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF533 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF533 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster

communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to `http://www.analog.com/dsp/tools/`.

ADSP-BF533 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The ADSP-BF533 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF533 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a users program to 20 KB of internal memory for code space with no restrictions for data space.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

The board features:

- Analog Devices ADSP-BF533 processor
  - Performance to 756 MHz
  - 160-pin Mini-BGA package
  - 27 MHz CLKIN oscillator
- Synchronous Dynamic Random Access Memory (SDRAM)
  - MT48LC32M16 - 64 MB (32M x 16 bits)
- Flash Memory
  - 2 MB (512K x 16 x 2chips)

- Analog Audio Interface
  - AD1836 – Analog Devices 96 kHz audio codec
  - 4 input RCA phono jacks (2 channels)
  - 6 output RCA phono jacks (3 channels)
- Analog Video Interface
  - ADV7183 video decoder w/ 3 input RCA phono jacks
  - ADV7171 video encoder w/ 3 output RCA phono jacks
- Universal Asynchronous Receiver/Transmitter (UART)
  - ADM3202 RS-232 line driver/receiver
  - `DB9` male connector
- LEDs
  - 10 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 6 general purpose (amber), and 1 USB monitor (amber)
- Push Buttons
  - 5 push buttons with debounce logic: 1 reset, 4 programmable flags
- Expansion Interface
  - `PPI`, `SPI`, `EBIU`, `Timers2-0`, `UART`, programmable flags, `SPORT0`, `SPORT1`
- Other Features
  - JTAG ICE 14-pin header

The EZ-KIT Lite board has two Flash memories with a total of 2 MB of memory. The Flash memories can be used to store user-specific boot code, allowing the board to run as a stand-alone unit. For more information, see "Flash Memory" on page 1-8. The board also has 64 MB of SDRAM, which can be used by the user at runtime.

SPORT0 interfaces with the AD1836 audio codec to aid development of audio signal processing applications. SPORT0 also attaches to an off-board connector for communication with other serial devices. For information about SPORT0, see "SPORT0 Audio Interface" on page 2-3.

The Parallel Peripheral Interface (PPI) of the processor connects to both a video encoder and video decoder, facilitating development of video signal processing applications.

The UART of the processor connects to an RS232 line driver and a DB9 male connector, providing an interface to a PC or other serial device.

Additionally, the EZ-KIT Lite board provides access to most of the processor's peripheral ports. Access is provided in the form of a three-connector expansion interface. For information about the expansion interface, see "Expansion Interface" on page 2-8.

Purpose of This Manual

The *ADSP-BF533 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes the operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF533 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

The product software installation is detailed in the *VisualDSP++ Installation Quick Reference Card*.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts (such as the *ADSP-BF533 Processor Hardware Reference* and the *Blackfin Processor Instruction Set Reference*) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and user's or getting started guides. For the locations of these documents, see "Related Documents".

Manual Contents

The manual consists of:

- Chapter 1, "Using EZ-KIT Lite" on page 1-1
  Describes the EZ-KIT Lite functionality from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components.
- Appendix A, "Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.

- Appendix B, "Schematics" on page B-1
  Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.

This appendix is not part of the online Help. The online Help viewers should go to the PDF version of the ADSP-BF533 EZ-KIT Lite Evaluation System Manual located in the `Docs\EZ-KIT Lite Manuals` folder on the installation CD to see the schematics. Alternatively, the schematics can be found on the Analog Devices Web site, `www.analog.com/processors`.

What's New in This Manual

This revision of the *ADSP-BF533 EZ-KIT Lite Evaluation System Manual* provides an updated listing of related documents and updated licensing information.

Technical or Customer Support

You can reach DSP Tools Support in the following ways.

- Visit the Embedded Processing and DSP products Web site at `http://www.analog.com/processors/technicalSupport`
- E-mail tools questions to `dsptools.support@analog.com`
- E-mail processor questions to `dsp.support@analog.com`
- Phone questions to **1-800-ANALOGD**

- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:

```
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
USA
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Supported Processors

This evaluation system supports Analog Devices ADSP-BF533 Blackfin processors.

Product Information

You can obtain product information from the Analog Devices Web site, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at `www.analog.com`. Our Web site provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit www.myanalog.com to sign up. Click **Register** to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

Processor Product Information

For information on embedded processors and DSPs, visit our Web site at www.analog.com/processors, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- E-mail questions or requests for information to
  dsp.support@analog.com
- Fax questions or requests for information to
  1-781-461-3010 (North America)
  +49 (89) 76 903-557 (Europe)
- Access the FTP Web site at
  ftp ftp.analog.com or ftp 137.71.23.21
  ftp://ftp.analog.com

Related Documents

For information on product related development software, see the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF533 Embedded Processor Datasheet	General functional description, pinout, and timing.
ADSP-BF533 Blackfin Processor Hardware Reference	Description of internal processor architecture and all register functions.
Blackfin Processor Instruction Set Reference	Description of all allowed processor assembly instructions.

Table 2. Related VisualDSP++ Publications

Title	Description
VisualDSP++ User's Guide	Description of VisualDSP++ features and usage.
VisualDSP++ Assembler and Preprocessor Manuals	Description of the assembler function and commands.
VisualDSP++ C/C++ Complier and Library Manual for Blackfin Processors	Description of the complier function and commands for Blackfin processors.
VisualDSP++ Linker and Utilities Manual	Description of the linker function and commands.
VisualDSP++ Loader Manual	Description of the loader/splitter function and commands.

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

All documentation is available online. Most documentation is available in printed form.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:

`http://www.analog.com/processors/resources/technicalLibrary`

Online Technical Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, the Dinkum Abridged C++ library, and Flexible License Manager (FlexLM) network license manager software documentation. You can easily search across the entire VisualDSP++ documentation set for any topic of interest. For easy printing, supplementary `.PDF` files of most manuals are provided in the `Docs` folder on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
`.CHM`	Help system files and manuals in Help format
`.HTM` or `.HTML`	Dinkum Abridged C++ library and FlexLM network license manager software documentation. Viewing and printing the `.HTML` files requires a browser, such as Internet Explorer 4.0 (or higher).
`.PDF`	VisualDSP++ and processor manuals in Portable Documentation Format (PDF). Viewing and printing the `.PDF` files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

If documentation is not installed on your system as part of the software installation, you can add it from the VisualDSP++ CD at any time by running the Tools installation. Access the online documentation from the VisualDSP++ environment, Windows® Explorer, or the Analog Devices Web site.

Accessing Documentation From VisualDSP++

To view VisualDSP++ Help, click on the **Help** menu item or go to the Windows task bar and navigate to the VisualDSP++ documentation via the **Start** menu.

To view ADSP-BF533 EZ-KIT Lite Help, which is part of the VisualDSP++ Help system, use the **Contents** or **Search** tab of the Help window.

Accessing Documentation From Windows

In addition to any shortcuts you may have constructed, there are many ways to open VisualDSP++ online Help or the supplementary documentation from Windows.

Help system files (`.CHM`) are located in the `Help` folder, and `.PDF` files are located in the `Docs` folder of your VisualDSP++ installation CD-ROM. The `Docs` folder also contains the Dinkum Abridged C++ library and the FlexLM network license manager software documentation.

Your software installation kit includes online Help as part of the Windows® interface. These help files provide information about VisualDSP++ and the ADSP-BF533 EZ-KIT Lite evaluation system.

Accessing Documentation From Web

Download manuals at the following Web site:
`http://www.analog.com/processors/resources/technicalLibrary/manuals`.

Select a processor family and book title. Download archive (`.ZIP`) files, one for each manual. Use any archive management software, such as WinZip, to decompress downloaded files.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**) and follow the prompts.

VisualDSP++ Documentation Set

To purchase VisualDSP++ manuals, call **1-603-883-2430**. The manuals may be purchased only as a kit.

If you do not have an account with Analog Devices, you are referred to Analog Devices distributors. For information on our distributors, log onto `http://www.analog.com/salesdir/continent.asp`.

Hardware Tools Manuals

To purchase EZ-KIT Lite and In-Circuit Emulator (ICE) manuals, call **1-603-883-2430**. The manuals may be ordered by title or by product number located on the back cover of each manual.

Processor Manuals

Hardware reference and instruction set reference manuals may be ordered through the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**), or downloaded from the Analog Devices Web site. Manuals may be ordered by title or by product number located on the back cover of each manual.

Data Sheets

All data sheets (preliminary and production) may be downloaded from the Analog Devices Web site. Only production (final) data sheets (Rev. 0, A, B, C, and so on) can be obtained from the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**); they also can be downloaded from the Web site.

To have a data sheet faxed to you, call the Analog Devices Faxback System at **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. If the data sheet you want is not listed, check for it on the Web site.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

Additional conventions, which apply only to specific chapters, may appear throughout this document.

1 USING EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-BF533 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "Audio Interface" on page 1-13
  Describes the board's audio interface.
- "Video Interface" on page 1-15
  Describes the board's video interface.
- "Example Programs" on page 1-16
  Provides information about the example programs included in the ADSP-BF533 EZ-KIT Lite evaluation system.
- "Background Telemetry Channel" on page 1-16
  Highlights the advantages of the Background Telemetry Channel feature of VisualDSP++.
- "VisualDSP++ Interface" on page 1-16
  Describes the trace, boot loading, context switching, and target options facilities of the EZ-KIT Lite system.

For more detailed information about programming the ADSP-BF533 Blackfin processor, see the documents referred to as "Related Documents".

Package Contents

Your ADSP-BF533 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF533 EZ-KIT Lite board
- *VisualDSP++ Installation Quick Reference Card*
- CD containing:
  - VisualDSP++ software
  - ADSP-BF533 EZ-KIT Lite debug software
  - USB driver files

  - Example programs
  - ADSP-BF533 *EZ-KIT Lite Evaluation System Manual* (this document)

- Universal 7.5V DC power supply
- USB 2.0 type cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF533 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before using the board.

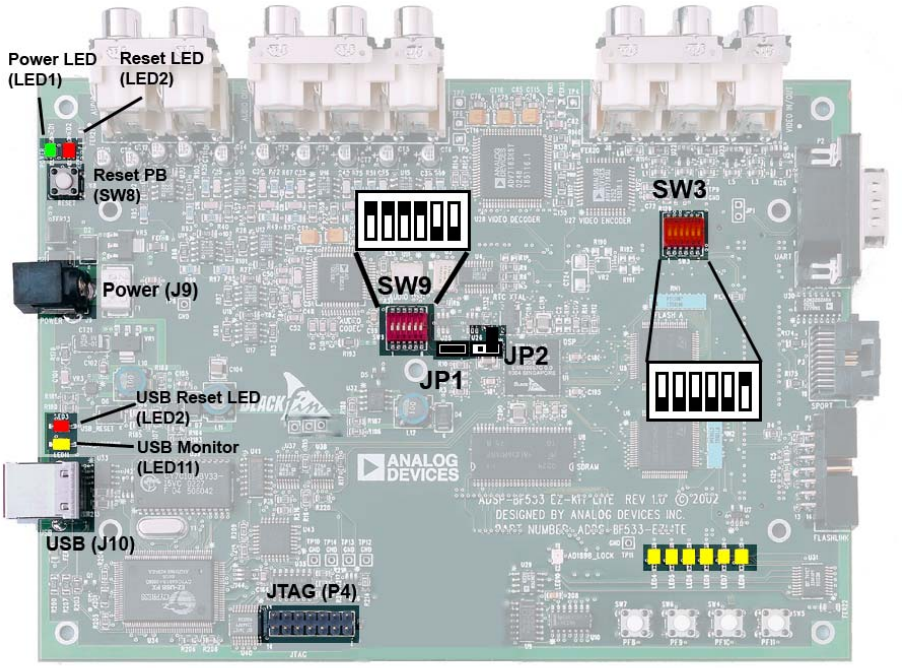

Figure 1-1. EZ-KIT Lite Hardware Setup

Installation Session Startup

For correct operation, install the software and hardware in the order presented in the *VisualDSP++ Installation Quick Reference Card*.

1. Verify that the yellow USB monitor LED (`LED11`, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. From the **Start** menu, navigate to the VisualDSP++ environment via the **Programs** menu.
   If you are running VisualDSP++ for the first time, the **New Session**

dialog box appears on the screen (skip the rest of the procedure and go to step 3).
If you have run VisualDSP++ previously, the last opened session appears on the screen.
To switch to another session, via the **Session List** dialog box, hold down the **Ctrl** key while starting VisualDSP++ (go to step 5).

3. In **Debug target**, select **EZ-KIT Lite (ADSP-BFxxx)**.
   In **Platform**, select **ADSP-BFxxx EZ-KIT Lite**.
   In **Processor**, choose the appropriate processor, **ADSP-BF533**.
   In **Session name**, type a new name or accept the default.
4. Click **OK** to return to the **Session List**.
5. Highlight the session and click **Activate**.

Evaluation License Restrictions

The ADSP-BF533 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF533 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a users program to 20 KB of internal memory for code space with no restrictions for data space.

The EZ-KIT Lite hardware must be connected and powered up to use VisualDSP++ with a valid evaluation or permanent license.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

Memory Map

The ADSP-BF533 processor has internal SRAM that can be used for instruction or data storage. The configuration of internal SRAM is detailed in the *ADSP-BF533 Processor Hardware Reference*.

The ADSP-BF533 EZ-KIT Lite board includes two types of external memory, SDRAM and flash memory.

The size of the SDRAM is 64 Mbytes (32M x 16-bits). The processor's memory select pin ~SMS0 is configured for the SDRAM.

The flash memory is implemented with two Dual-Bank flash memory devices. These devices include primary and secondary flash memory as well as internal SRAM and registers. Primary flash memory totals 2 Mbytes mapped into two separate asynchronous memory banks, 1 Mbyte each. Secondary flash memory, along with SRAM and registers, occupies the third bank of asynchronous memory space. The processor's ~AMS0, ~AMS1, and ~AMS2 memory select pins are used for that purpose.

Table 1-1. EZ-KIT Lite Evaluation Board Memory Map

Start Address		End Address	Content
External Memory	0x0000 0000	0x07FF FFFF	SDRAM Bank 0 (SDRAM). See "SDRAM Interface" on page 1-7.
	0x2000 0000	0x200F FFFF	ASYNC Memory Bank 0 (Primary Flash A). See "Flash Memory" on page 1-8.
	0x2010 0000	0x201F FFFF	ASYNC Memory Bank 1 (Primary Flash B). See "Flash Memory" on page 1-8.
	0x2020 0000	0x202F FFFF	ASYNC Memory Bank 2 (Flash A and B Secondary Memory, SRAM and Internal Registers). See "Flash Memory" on page 1-8.
	All other locations		Not used

Table 1-1. EZ-KIT Lite Evaluation Board Memory Map (Cont'd)

Start Address		End Address	Content
Internal Memory	0xFF80 0000	0xFF80 3FFF	Data Bank A SRAM 16 KB
	0xFF80 4000	0xFF80 7FFF	Data Bank A SRAM/CACHE 16 KB
	0xFF90 0000	0xFF90 3FFF	Data Bank B SRAM 16 KB
	0xFF90 4000	0xFF90 7FFF	Data Bank B SRAM/CACHE 16 KB
	0xFFA0 0000	0xFFA0 FFFF	Instruction SRAM 64 KB
	0xFFA1 0000	0xFFA1 3FFF	Instruction SRAM /CACHE 16 KB
	0xFFB0 0000	0xFFB0 0FFF	Scratch Pad SRAM 4 KB
	0xFFC0 0000	0xFFDF FFFF	System MMRs 2 MB
	0xFFE0 0000	0xFFFF FFFF	Core MMRs 2 MB
	All other locations		Reserved

SDRAM Interface

The three SDRAM control registers must be initialized in order to use the MT48LC32M16 - 64 MB (32M x 16 bits) SDRAM memory.

If you are in an EZ-KIT Lite or emulator session, the SDRAM registers are set to the values in Table 1-2 automatically when a reset operation is performed. Clearing the **Use XML reset values** check box on the **Target Options** dialog box, which is accessible through the **Settings** pull-down menu, disables this feature. For more information see the "Target Options" on page 1-18.The numbers were derived for maximum flexibility and work for a system clock frequency between 54 MHz and 133 MHz.

Automatic configuration of SDRAM is not optimized for any SCLK frequency. Table 1-2 shows the optimized configuration for the SDRAM registers using a 118.8 MHz, 126 MHz, and 133 MHz SCLK. The fre-

quency of 118.8 MHz is the maximum SCLK frequency when using a 594 MHz core frequency, the maximum frequency for the EZ-KIT Lite when using the internal voltage regulator. Only the `EBIU_SDRRC` register needs to be modified in the user code to achieve maximum performance.

Table 1-2. SDRAM Optimum Settings

Register	SCLK = 133 MHz (Processor MAX)	SCLK = 126 MHz (CCLK = 756 MHz)	SCLK = 118.8 MHz (CCLK = 594 MHz)
EBIU_SDGCTL	0x0091 998D	0x0091 998D	0x0091 998D
EBIU_SDBCTL	0x0000 0025	0x0000 0025	0x0000 0025
EBIU_SDRRC	0x0000 0406	0x0000 03CF	0x0000 0397

An example program is included in the EZ-KIT installation directory to demonstrate how to set up the SDRAM interface.

Flash Memory

The following sections describe how to use the memory and general-purpose IO pins, as well as how to configure the flash memory device.

The ADSP-BF533 EZ-KIT Lite board employs two PSD4256G6V Flash/General-Purpose IO devices from STMicroelectronics. These devices not only have flash memory but also extra IO pins, which are memory mapped.

Example code is provided in the EZ-KIT installation directory to demonstrate how to program the flash memory as well as to demonstrate the functionality of the general-purpose IO pins.

Flash Memory Map

Each device includes the following memory segments:

- 1M byte of primary flash memory
- 64K bytes of secondary flash memory
- 32 Kbytes of internal SRAM
- 256 Bytes of configuration registers (IO control)

Access to each segment can be 8-bit or 16-bit. The processor's ~AMS0, ~AMS1, and ~AMS2 memory select pin are used for that purpose. Asynchronous memory Bank 0 is always enabled after a hard reset, while Banks 1 and 2 need to be enabled by software. Table 1-3 provides an example on asynchronous memory configuration registers.

Table 1-3. Asynchronous Memory Control Registers Settings Example

Register	Value	Function
EBIU_AMBCTL0	0x7BB07BB0	Timing control for Banks 1 and 0
EBIU_AMBCTL1 bits 15-0	0x7BB0	Timing control for Bank 2 (Bank 3 is not used)
EBIU_AMGCTL bits 3-0	0xF	Enable all banks

Each flash chip is initially configured with the memory sectors mapped into the processor's address space as shown in Table 1-4.

Table 1-4. Flash Memory Map

Start Address	End Address	Content
0x2000 0000	0x200F FFFF	Flash A Primary (1MB)
0x2010 0000	0x201F FFFF	Flash B Primary (1MB)
0x2020 0000	0x2020 FFFF	Flash A Secondary (64KB)

Table 1-4. Flash Memory Map (Cont'd)

Start Address	End Address	Content
0x2024 0000	0x2024 7FFF	Flash A SRAM (32KB)
0x2027 0000	0x2027 00FF	Flash A Registers (256 Bytes)
0x2028 0000	0x2028 FFFF	Flash B Secondary (64KB)
0x202C 0000	0x202C 7FFF	Flash B SRAM (32KB)
0x202E 0000	0x202E 00FF	Flash B Registers (256 Bytes)
All other locations		Reserved

Flash General-Purpose IO

This section describes general-purpose IO signals that are controlled by means of setting appropriate registers of the Flash A or Flash B. These registers are mapped into the processor's address space, as shown in Table 1-4.

Flash device IO pins are arranged as 8-bit ports labeled `A` through `G`. There is a set of 8-bit registers associated with each port. These registers are: `Direction`, `Data In`, and `Data Out`. Note that the `Direction` and `Data Out` registers are cleared to all zeros at power-up or hardware reset.

The `Direction` register controls IO pins direction. When a bit is `0`, a corresponding pin functions as an input. When the bit is `1`, a corresponding pin is an output. This is a 8-bit read-write register.

The `Data In` register allows reading the status of port's pins. This is a 8-bit read-only register.

The `Data Out` register allows clearing an output pin to `0` or setting it to `1`. This is a 8-bit read-write register.

The ADSP-BF533 EZ-KIT Lite board employs only Flash A and Flash B ports A and B. Table 1-5 and Table 1-6 provide configuration register addresses for Flash A and Flash B, respectively (only ports A and B are listed). The following bits connect to the Expansion Board connector.

- Flash A port B bits 7 and 6
- Flash B port A bits 7-0 and port B bits 7-0

Table 1-5. Flash A Configuration Registers for Port A, B

Register Name	Port A Address	Port B Address
Data In (Read-only)	0x2027 0000	0x2027 0001
Data Out (Read-Write)	0x2027 0004	0x2027 0005
Direction (Read-Write)	0x2027 0006	0x2027 0007

Table 1-6. Flash B Configuration Registers for Port A, B

Register Name	Port A Address	Port B Address
Data In (Read-only)	0x202E 0000	0x202E 0001
Data Out (Read-Write)	0x202E 0004	0x202E 0005
Direction (Read-Write)	0x202E 0006	0x202E 0007

Table 1-7 and Table 1-8 depict the IO assignments.

Table 1-7. Flash A Port A Controls

Bit #	User IO	Bit Value
7	Not defined	Any
6	Not defined	Any
5	PPI Clock Select bit 1	00 = Local OSC (27 MHz)
4	PPI Clock Select bit 0	01= Video Decoder Pixel Clock 1X = Expansion Board PPI Clock

Table 1-7. Flash A Port A Controls (Cont'd)

Bit #	User IO	Bit Value
3	Video Decoder Reset	0= Reset ON; 1= Reset OFF
2	Video Encoder Reset	0= Reset ON; 1= Reset OFF
1	Reserved	Any
0	Codec Reset	0= Reset ON; 1= Reset OFF

Table 1-8. Flash A Port B Controls

Bit #	User IO	Bit Value
7	Not used	Any
6	Not used	Any
5	LED9	0= LED OFF; 1= LED ON
4	LED8	0= LED OFF; 1= LED ON
3	LED7	0= LED OFF; 1= LED ON
2	LED6	0= LED OFF; 1= LED ON
1	LED5	0= LED OFF; 1= LED ON
0	LED4	0= LED OFF; 1= LED ON

Configuring Flash Memory

The flash memory is completely configurable. To modify the default setup of each flash, you must use PSDsoft Express™ software. After the project has been modified, the flash memory must be re-programmed using FlashLINK™. The default project file is provided in `\…\Blackfin\EZ-KITs\ADSP-BF533\PSDConfigFiles` directory. Analog Devices does not provide any support for setting up the PSD4256G6V with PSDsoft Express or programming it using FlashLINK. Email STMicroelectronics at `apps.psd@st.com` for technical assistance.

The PSD4256G6Vcan be re-programmed using the FlashLINK JTAG programming cable available from STMicroelectronics (www.st.com/psd) for approximately $59. FlashLINK plugs into any PC parallel port. The PSDsoft Express development software is required to modify the DSM2150 configuration and to operate the FlashLINK cable. PSDsoft Express can be downloaded at no charge from www.st.com/psd.

LEDs and Push Buttons

The EZ-KIT Lite provides four push buttons and six LEDs for general-purpose IO.

The six LEDs, labeled LED4 through LED9, are accessed via some of the general-purpose IO pins of flash memory interface. For information on how to program the pins, see "Flash General-Purpose IO" on page 1-10.

The four general-purpose push button are labeled SW4 through SW7. A status of each individual button can be read through programmable flag (PF) inputs, PF8 through PF11. A PF reads "1" when a corresponding switch is being pressed-on. When the switch is released, the PF reads "0". A connection between the push button and PF input is established through the SW9 DIP switch. See "Push Button Enable Switch (SW9)" on page 2-11 for details.

An example program is included in the EZ-KIT installation directory to demonstrate the functionality of the LEDs and push buttons.

Audio Interface

The AD1836 audio codec provides three channels of stereo audio output and two channels of multichannel 96 kHz input. The SPORT0 interface of the processor is linked with the stereo audio data input and output pins of

the AD1836 codec. The processor is capable of transferring data to the audio codec in time-division multiplexed (TDM) or Two-Wire Interface (TWI) mode.

The TWI mode allows the codec to operate with a 96 kHz sample rate but only allows you to use two channels of output. TDM mode can operate at a maximum of 48 kHz sample rate but allows for simultaneous use of all input and output channels. When using TWI mode, the TSCLK0 and RSCLK0 pins, as well as the TFS0 and RFS0 pins of the processor, must be tied together external to the processor. This is accomplished with the SW9 DIP switch (see "Push Button Enable Switch (SW9)" on page 2-11 for more information).

The AD1836 audio codec's internal configuration registers are configured using the processor's SPI port. The processor's PF4 programmable flag pin is used as the select for this device. For information on how to configure the multichannel codec, go to www.analog.com/UploadedFiles/Datasheets/344740003AD1836_prc.pdf.

The reset for the AD1836 codec comes from the general-purpose IO pin PA0 of Flash A. For information on how to use the pin, see "Flash General-Purpose IO" on page 1-10.

Example programs are included in the EZ-KIT installation directory to demonstrate the AD1836 codec operation.

Video Interface

The board supports video input and output applications. The ADV7171 video encoder provides up to three output channels of analog video, while the ADV7183 video decoder provides up to three input channels of analog video. Both the encoder and the decoder connect to the Parallel Peripheral Interface (PPI) of the ADSP-BF533 processor. For additional information on the video interface hardware, refer to "PPI Interface" on page 2-5.

For the video interface to be operational, the following basic steps must be performed.

1. Configure the SW3 DIP switch as required by the application. Refer to "Video Configuration Switch (SW3)" on page 2-10 for details.
2. Remove reset to the video device. Refer to "Flash General-Purpose IO" on page 1-10 for details.
3. If using the decoder:
   - Enable device by driving programmable flag output PF2 to "0".
   - Select PPI clock (see Table 1-7 on page 1-11).
4. Program internal registers of the video device in use. Both video encoder and decoder use a 2-wire serial interface to access internal registers. A programmable flag PF0 functions as a serial clock (SCL), and PF1 functions as a serial data (SDAT).
5. Program the ADSP-BF533 processor's PPI interface (configuration registers, DMA, etc.).

Example programs are included in the EZ-KIT installation directory to demonstrate the capabilities of the video interface.

Example Programs

Example programs are provided with the ADSP-BF533 EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in the `\…\Blackfin\EZ-KITs\ADSP-BF533\Examples` subdirectory of the VisualDSP++ installation directory. Please refer to the readme file provided with each example for more information.

Background Telemetry Channel

The ADSP-BF533 USB debug agent supports the Background Telemetry Channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting processor execution.

The BTC allows the user to view a variable as it is updated or changed, all while the processor continues to execute. For increased performance of the BTC, including faster reading and writing, please check out our latest line of processor emulators at `www.analog.com/Analog_Root/productPage/productHome/0,2121,EMULATORS,00.html`. For more information about the Background Telemetry Channel, see the *VisualDSP++ User's Guide* or online Help.

VisualDSP++ Interface

This section provides information on the following parts of the VisualDSP++ graphical user interface:

- "Restricted Software Breakpoints" on page 1-20

Trace Window

Choosing the **Trace** command from the **View–>Debug Windows** menu opens the **Trace** window (Figure 1-2).

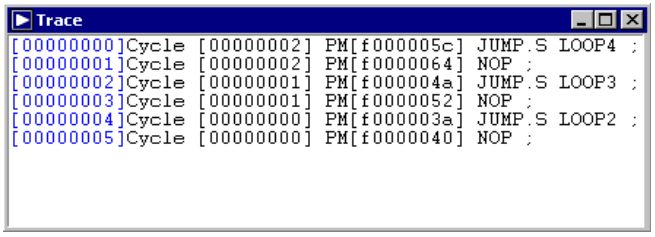

Figure 1-2. Trace Window

The trace buffer stores a history of the last 16 changes in program flow taken by the program sequencer. View the history to recreate the program sequencer's most recent path.

The trace buffer does not track changes in flow caused by zero-overhead loops or while in the reset service routine.

To use the trace buffer, ensure your program leaves the reset service routine.

Enabling Trace Buffer

To view trace history in the **Trace** window, first, enable the trace buffer (choose **Enable Trace** from the **Tools–>Trace** menu). On each halt, the **Trace** window is updated with the changes that occurred since the last halt. Reading the trace buffer destroys the trace buffer's contents and discards the information previously stored before the last run.

Reading Trace Buffer Data

The first column between the square brackets (in blue) indicates the line number in the **Trace** window.

The second column between square brackets, which comes in vertical pairs, shows the trace number. For each discontinuity, the first (top position) is the source trace, and the second (bottom position) is the destination trace. The third column in between square brackets shows the addresses of the instructions. Each address is followed by the assembly instruction.

The trace grows upward. In Figure 1-2, trace 0 occurred before trace 1, which occurred before trace 2, and so on.

Boot Load

Choosing **Boot Load** from the **Settings** menu runs the processor and performs a hard reset on the board. This command saves you from having to shut down VisualDSP++, reset the EZ-KIT Lite board, and bring up VisualDSP++ again when you want to perform a hard reset.

Use this feature when loading debug boot code from an external part or when you want to put the device into a known state.

Target Options

Choosing **Target Options** from the **Settings** menu opens the **Target Options** dialog box (Figure 1-3). Use target options to control certain aspects of the processor on the ADSP-BF533 EZ-KIT Lite evaluation system.

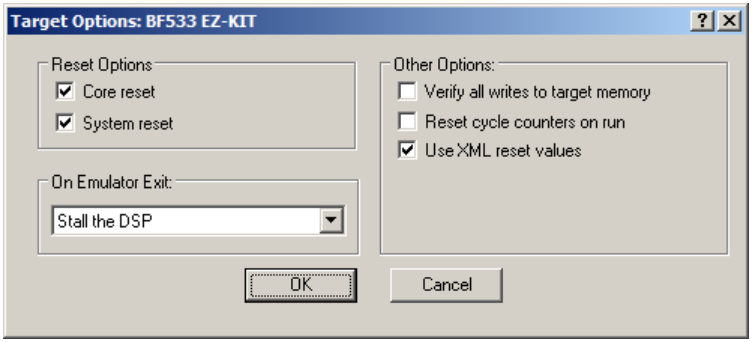

Figure 1-3. Target Options Dialog Box

Reset Options

Reset options control how the processor behaves when a reset occurs. The reset options are described in Table 1-9.

Table 1-9. Reset Options

Option	Description
Core reset	Resets the core when the debugger executes a reset.
System reset	Resets the peripherals when the debugger executes a reset.

On Emulator Exit

This target option controls processor behavior when VisualDSP++ relinquishes processor control (for example, when exiting VisualDSP++). The option is described in Table 1-10.

Other Options

Table 1-11 describes other available target options.

Table 1-10. On Emulator Exit Target Options

Option	Description
On Emulator Exit	Determines the state the processor is left in when the emulator relinquishes control of the processor: **Reset DSP and Run** causes the processor to reset and begin execution from its reset vector location. **Run from current PC** causes the processor to begin running from its current location. **Stall the DSP** resets the processor and then writes a `JUMP 0` to the first location in internal memory so the processor is stuck in a tight loop after exiting.

Table 1-11. Miscellaneous Target Options

Option	Description
Verify all writes to target memory	Validates all memory writes to the processor. After each write, a read is performed and the values are checked for a matching condition. Enable this option during initial program development to locate and fix initial build problems (such as attempting to load data into non-existent memory). Clear this option to increase performance while loading executable files, since VisualDSP++ does not perform the extra reads that are required to verify each write.
Reset cycle counters on run	Resets the cycle count registers to zero before a Run command is issued. Select this option to count the number of cycles executed between breakpoints in a program.
Use XML reset values	Uses a section in the processor-specific `.XML` file located in the installation's `system` folder. The file defines registers that are reset to certain values. The values are read at startup and subsequently used to set the registers when a reset is performed through VisualDSP++.

Restricted Software Breakpoints

The EZ-KIT Lite development system restricts breakpoint placement when certain conditions are met. That is, under some conditions, breakpoints cannot be placed effectively. Such conditions depend on bus architecture, pipeline

depth, and ordering of the EZ-KIT Lite and its target processor.

2 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF533 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the configuration of the ADSP-BF533 EZ-KIT Lite board and explains how the board components interface with the processor.
- "Jumper and Switch Settings" on page 2-9
  Shows the location and describes the function of the configuration jumpers and switches.
- "LEDs and Push Buttons" on page 2-13
  Shows the location and describes the function of the LEDs and push buttons.
- "Connectors" on page 2-16
  Shows the location and gives the part number for all of the connectors on the board. Also, the manufacturer and part number information is given for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

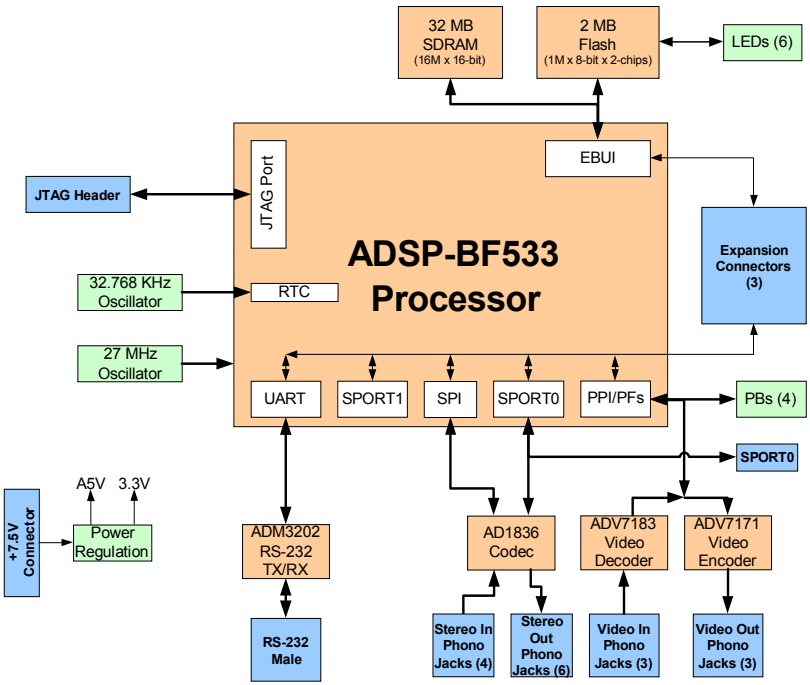

Figure 2-1. System Architecture

The EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-BF533 Blackfin processor. The processor has IO voltage of 3.3V. The core voltage is derived from this 3.3v supply and uses the internal regulator of the processor. The core voltage and the core clock rate can be set on the fly by the processor. Refer to the *Hardware Reference Manual* for more information.

The default mode for the processor is flash boot. See "Boot Mode Select Jumpers (JP2–1)" on page 2-10 for information about changing the default boot mode.

External Bus Interface Unit

The External Bus Interface Unit (EBIU) connects an external memory to the ADSP-BF533 device. It includes a 16-bit wide data bus, an address bus, and a control bus. Both 16-bit and 8-bit access are supported. On the EZ-KIT Lite, the EBI unit connects to SDRAM and flash memory.

64 MB (32M x 16 bits) of SDRAM connect to the synchronous memory select 0 pin (~SMS0). Refer to "SDRAM Interface" on page 1-7 for information about configuring the SDRAM. Note that SDRAM clock is the processor's Clock Out (CLK OUT), which frequency should not exceed 133 MHz.

Two flash memory devices are connected to the asynchronous memory select signals, ~AMS2 through ~AMS0. The devices provide total of 2 Mbytes of primary flash memory, 128 Kbytes of secondary flash memory, and 64 Kbytes of SRAM. The processor can use this memory for both booting and storing information during normal operation. Refer to "Flash Memory" on page 1-8 for details.

All of the address, data, and control signals are available externally via the extender connectors P3-1. The pinout of these connectors can be found in Appendix B, "Schematics" on page B-1.

SPORT0 Audio Interface

The SPORT0 interface is connected to the AD1836 audio codec, the SPORT connector (P3), and the expansion interface. The AD1836 codec uses both the primary and secondary data transmit and receive pins to input and output data from the audio input and outputs.

The pinout of the SPORT connector and the expansion interface connectors can be found in Appendix B, "Schematics" on page B-1.

SPI Interface

The processor's Serial Peripheral Interconnect (SPI) interface is connected to the AD1836 audio codec and the expansion interface. The SPI connection to the AD1836 is used to access the control registers of the device. The PF4 flag of the processor is used as the devices select for the SPI port.

Programmable Flags

The processor has 15 programmable flag pins (PFs). The pins have multiple functions, depending on the setup of the processor. Table 2-1 shows how the programmable flag pins are used on the EZ-KIT Lite.

Table 2-1. Programmable Flag Connections

Processor PF Pin	Other Processor Function	EZ-KIT Function
PF0		Serial clock for programming ADV7171 and ADV7183
PF1		Serial data for programming ADV7171 and ADV7183
PF2		ADV7183 ~OE
PF3	FS3	ADV7183 Field Pin. See "Video Configuration Switch (SW3)" on page 2-10.
PF4		AD1836 SPI Select
PF5		
PF6		
PF7		

Table 2-1. Programmable Flag Connections (Cont'd)

Processor PF Pin	Other Processor Function	EZ-KIT Function
PF8		Push button (SW4). See "LEDs and Push Buttons" on page 1-13 and "Push Button Enable Switch (SW9)" on page 2-11 for information on how to disable the push button.
PF9		Push button (SW5). See "LEDs and Push Buttons" on page 1-13 and "Push Button Enable Switch (SW9)" on page 2-11 for information on how to disable the push button.
PF10		Push button (SW6). See "LEDs and Push Buttons" on page 1-13 and "Push Button Enable Switch (SW9)" on page 2-11 for information on how to disable the push button.
PF11		Push button (SW7). See "LEDs and Push Buttons" on page 1-13 and "Push Button Enable Switch (SW9)" on page 2-11 for information on how to disable the push button.
PF12	PPI7	ADV7171 and ADV7183 Data (MSB)
PF13	PPI6	ADV7171 and ADV7183 Data
PF14	PPI5	ADV7171 and ADV7183 Data
PF15	PPI4	ADV7171 and ADV7183 Data

PPI Interface

The Parallel Peripheral Interface (PPI) of the ADSP-BF533 processor is a half-duplex, bi-directional port that can accommodate up to 16 bits of data. The interface has a dedicated input clock (27 MHz), three multiplexed frame sync signals, and four bits of dedicated data. The remaining data bits come from re-configured programmable flag pins. For information about the pins, which multiplexed with the PPI, see "Programmable Flags" on page 2-4. For information about the ADSP-BF533 processor

PPI interface, refer to the *ADSP-BF533 Blackfin Processor Hardware Reference*. Table 2-2 describes the PPI pins and their use on the EZ-KIT Lite board.

Table 2-2. PPI Connections

Processor PPI Pin	Other Processor Function	EZ-KIT Function
PPI7	PF12	ADV7171 and ADV7183 Data (MSB)
PPI6	PF13	ADV7171 and ADV7183 Data
PPI5	PF14	ADV7171 and ADV7183 Data
PPI4	PF15	ADV7171 and ADV7183 Data
PPI3		ADV7171 and ADV7183 Data
PPI2		ADV7171 and ADV7183 Data
PPI1		ADV7171 and ADV7183 Data
PPI0		ADV7171 and ADV7183 Data
PF3	FS3	ADV7183 Field Pin. For more information, see "Video Configuration Switch (SW3)" on page 2-10.
TMR1	PPI_HSYNC	ADV7171 and ADV7183 HSYNC. For more information, see "Video Configuration Switch (SW3)" on page 2-10.
TMR2	PPI_FSYNC	ADV7171 and ADV7183 VSYNC. For more information, see "Video Configuration Switch (SW3)" on page 2-10.
PPI_CLK		Input from either the ADV7183 output clock or the same 27 MHz oscillator driving the processor. For more information, see "Video Interface" on page 1-15.

The ADSP-BF533 EZ-KIT Lite board employs 8-bit PPI interface for video output and video input.

Video Output Mode

In the video output mode, the PPI interface is configured as output and connects to the on-board video encoder device, ADV7171. The ADV7171 encoder device generates three analog video channels on DAC B, DAC C, and DAC D outputs. The PPI data connects to P7-0 of the encoder's pixel inputs. The encoder's PPI input clock runs at 27 MHz, and it is in phase with CLK IN of the ADSP-BF533 processor.

The encoder's synchronization signals, HSYNC and VSYNC, can be configured as inputs or outputs. Video Blanking control signal is at level "1". The HSYNC and VSYNC signals can be connected to the ADSP-BF533 processor's multiplexed sync pins and to the on-board video decoder, ADV7183, via the SW3 switch, as described in "Video Configuration Switch (SW3)" on page 2-10.

Video Input Mode

In the video input mode, the PPI interface is configured as input and connects to the on-board video decoder device, ADV7183. The ADV7183 decoder receives three analog video channels on AIN1, AIN4, and AIN5 input. The decoder's pixel data outputs P15-8 drive the PPI data (PPI3-0 and PF15-12). The decoder's 27 MHz pixel clock output can be selected to drive PPI clock, as shown in Table 1-7 on page 1-11.

Synchronization outputs of the decoder, HS/HACTIVE, VS/VACTIVE, and FIELD can connected to the ADSP-BF533 processor's multiplexed sync pins and to the on-board video encoder, ADV7171, via the SW3 DIP switch, as described in "Video Configuration Switch (SW3)" on page 2-10.

UART Port

The processor' Universal Asynchronous Receiver/Transmitter (UART) port is connected to the ADM3202 RS232 line driver as well as to the expansion interface. The RS232 line driver is connected to the DB9 male connector, allowing you to interface with a PC or other serial device.

Expansion Interface

The expansion interface consists of the three 90-pin connectors. Table 2-3 on page 2-8 shows the interfaces each connector provides. For the exact pinout of these connectors, refer to Appendix B, "Schematics" on page B-1. The mechanical dimensions of the connectors can be obtained from Technical or Customer Support.

Table 2-3. Connector Interfaces

Connector	Interfaces
J1	5V, G ND, Address, Data, PPI
J2	3.3V, GND, SPI, NMI, TMR2–0, SPORT0, SPORT1, PF15–0, EBUI control signals
J3	5V, 3.3V, GND, UART, Flash IO, Reset, Video control signals

Limits to the current and to the interface speed must be taken into consideration when you use the expansion interface. The maximum current limit is dependent on the capabilities of the regulator used. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a 6-pin interface. The JTAG emulation port of the processor is also connected to the USB debugging interface. When an emulator is connected to the board at P4, the USB debugging interface is disabled. See "JTAG (P4)" on page 2-20 for more information about the JTAG connector.

To learn more about available emulators, contact Analog Devices (see "Product Information").

Jumper and Switch Settings

This section describes the operation of the jumpers and DIP switches. The jumpers and switch locations are shown in Figure 2-2.

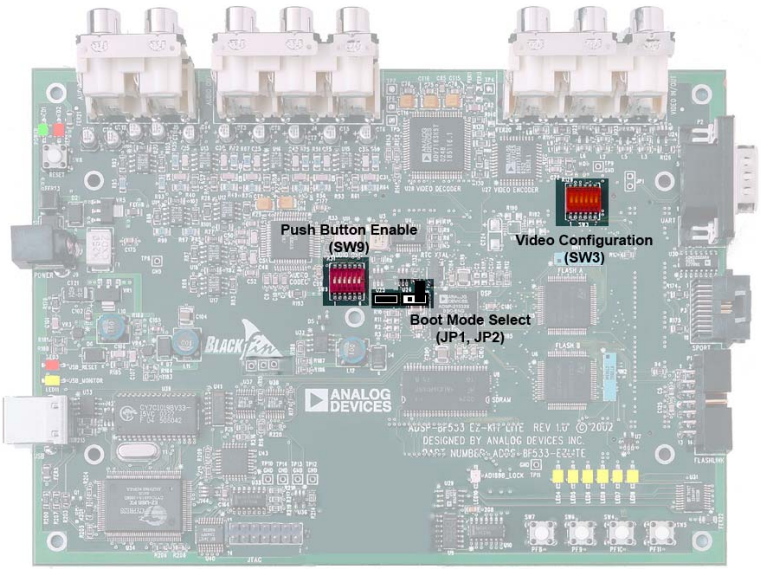

Figure 2-2. Jumper and Switch Locations

Boot Mode Select Jumpers (JP2–1)

The JP1 and JP2 jumpers determine the boot mode of the processor. Table 2-4 shows the available boot mode settings. By default, the processor boots from the on-board flash memory.

Table 2-4. Boot Mode Settings

JP1 (BMODE1)	JP2 (BMODE0)	Boot Mode
Installed	Installed	16-Bit External Memory
Installed [1]	**Not installed**	**Flash Memory**
Not installed	Installed	Reserved
Not installed	Not installed	SPI EEPROM

1 Default settings

Test DIP Switches (SW2–1)

Two DIP switches (SW1 and SW2) are located on the bottom of the board. The switches are used only for testing and should always be in the "OFF" position.

Video Configuration Switch (SW3)

The video configuration switch (SW3) controls how some video signals from the ADV7183 video decoder and ADV7171 video encoder are routed to the processor's PPI. The switch also determines if the PF2 pin controls the OE of the ADV7183 video decoder outputs. Table 2-5 shows which processor's signals are connected to the encoder and decoder when in the "ON" position.

Table 2-5. Video Configuration Switch (SW3)

Switch Position (Default)	Processor Signal	Video Signal
1 (OFF)	TMR1 (HSYNC)	HSYNC (ADV7171)
2 (OFF)	TMR1 (HSYNC)	HS (ADV7183)
3 (OFF)	TMR2 (VSYNC)	VS (ADV7183)
4 (OFF)	TMR2 (VSYNC)	VSYNC (ADV7171)
5 (OFF)	PF3 (FIELD)	FIELD (ADV7183)
6 (ON)	PF2	~OE (ADV7183)

Positions 1 thorough 5 of SW3 determine how and if the VSYNC, HSYNC, and FIELD control signals are routed to the processors PPI. In standard configuration of the encoder and decoder, this is not necessary because the processor is capable of reading the embedded control information, which is in the data stream.

Position 6 of SW3 determines whether PF2 is connected to the ~OE signal of the ADV7183. When the switch "OFF", PF2 can be used for other operations, and the decoder output enable is held "HIGH" with a pull-up resistor.

Push Button Enable Switch (SW9)

The push button enable switch (SW9) positions 1 through 4 allow the user to disconnect the drivers associated with the push buttons from the PF pins of the processor. Positions 5 and 6 are used to connect the transmit and receive the frame syncs and clocks of SPORT0. This is important when the AD1836 video decoder and the processor are communicating in I^2S mode. Table 2-6 shows which PF is driven when the switch is in the "ON" position.

Table 2-6. Push Button Enable Switch (SW9)

Switch Position	Default Setting	Pin #	Signal (Side 1)	Pin #	Signal (Side 2)
1	ON	1	SW4	12	PF8
2	ON	2	SW5	11	PF9
3	ON	3	SW6	10	PF10
4	ON	4	SW7	9	PF11
5	OFF	5	TFS0	8	RFS0
6	OFF	6	RSCLK0	7	TSCLK0

LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 2-3 shows the locations of the LEDs and push buttons.

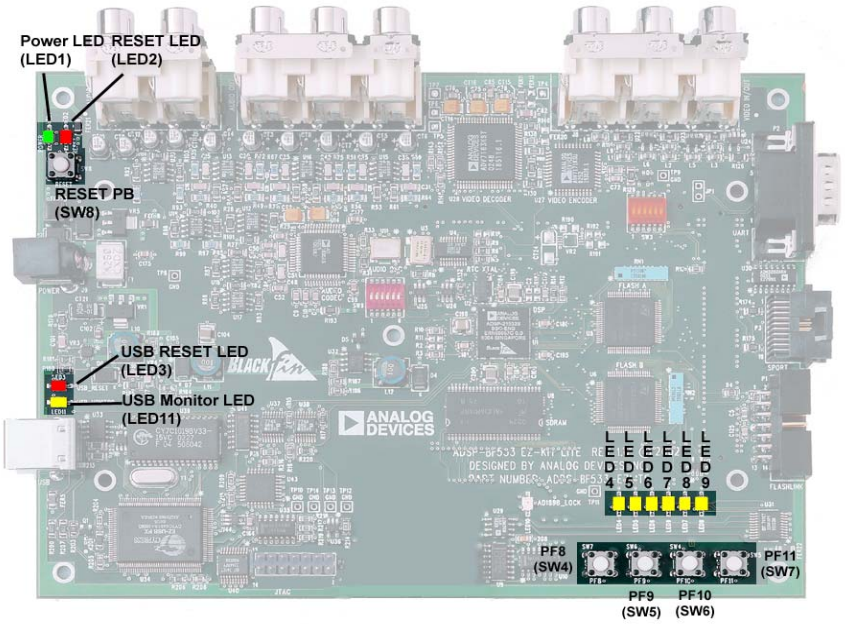

Figure 2-3. LED and Push Button Locations

Programmable Flag Push Buttons (SW7–4)

Four push buttons, `SW7-4`, are provided for general-purpose user input. The buttons connect to the processor's programmable flag pins `PF11-8`. The push buttons are active "`HIGH`" and, when pressed, send a `High (1)` to the processor. Refer to "LEDs and Push Buttons" on page 1-13 for more information on how to use the PFs when programming the processor. The push button enable switch (`SW9`) is capable of disconnecting the push but-

tons from the PF (refer to "Push Button Enable Switch (SW9)" on page 2-11 for more information). The programmable flag signals and their corresponding switches are shown in Table 2-7.

Table 2-7. Programmable Flag Switches

Processor Programmable Flag Pin	Push Button Reference Designator
PF8	SW4
PF9	SW5
PF10	SW6
PF11	SW7

Reset Push Button (SW8)

The RESET push button resets all of the ICs on the board. One exception is the USB interface chip (U34). The chip is not being reset when the push button is pressed after the USB cable has been plugged in and communication has been correctly initialized with the PC. After USB communication has been initialized, the only way to reset the USB is by powering down the board.

Power LED (LED1)

When LED1 is lit (green), it indicates that power is being properly supplied to the board.

Reset LEDs (LED3–2)

When LED2 is lit, it indicates that the master reset of all the major ICs is active. When LED3 is lit, the USB interface chip (U34) is being reset. The USB chips only reset on power-up, or if USB communication has not been initialized.

User LEDs (LED9–4)

Six LEDs are connected to six of the flash memory (U5) general-purpose IO pins. The LEDs are active "HIGH" and are lit by writing a "1" to the correct memory address in the flash memory. Refer to "LEDs and Push Buttons" on page 1-13 for more information about how to use the flash when programming the LEDs.

Table 2-8. User LEDs

LED Reference Designator	Flash Port Name
LED4	PB0
LED5	PB1
LED6	PB2
LED7	PB3
LED8	PB4
LED9	PB5

USB Monitor LED (LED11)

The USB Monitor LED (LED11) indicates that USB communication has been initialized successfully and you may connect to the processor using a VisualDSP++ EZ-KIT Lite session. This should take approximately 15 seconds. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver.

When VisualDSP++ is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Connectors

This section describes the connector functionality and provides information about mating connectors. The locations of the connectors are shown in Figure 2-4.

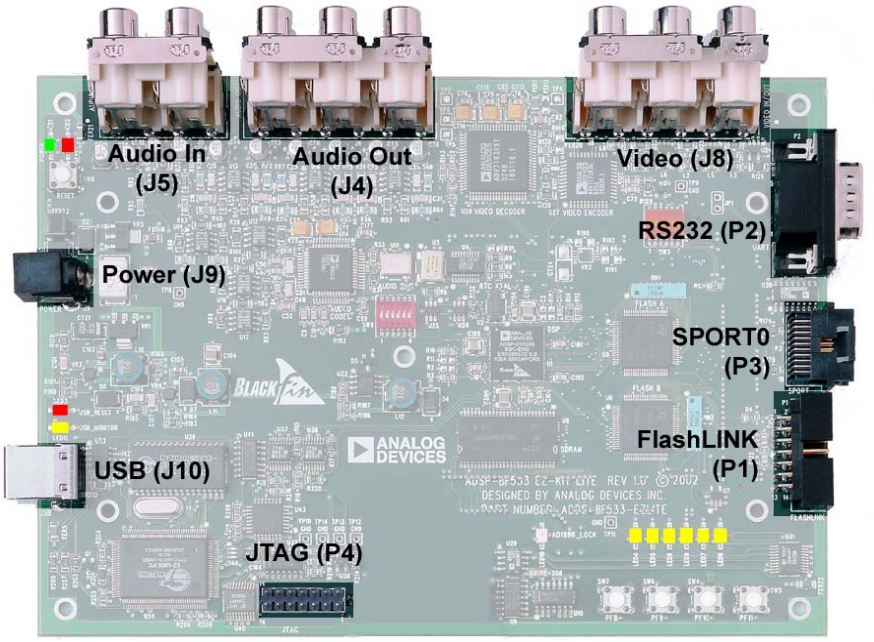

Figure 2-4. Connector Locations

Expansion Interface (J3–1)

Three board-to-board connector footprints provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the expansion interface, see on page 2-8. For the availability and pricing of the J1, J2, and J3 connectors, contact Samtec.

Part Description	Manufacturer	Part Number
90 Position 0.05" Spacing, SMT (J1, J2, J3)	Samtec	SFC-145-T2-F-D-A
Mating Connector		
90 Position 0.05” Spacing (Through Hole)	Samtec	TFM-145-x1 Series
90 Position 0.05” Spacing (Surface Mount)	Samtec	TFM-145-x2 Series
90 Position 0.05” Spacing (Low Cost)	Samtec	TFC-145 Series

Audio (J5–4)

Part Description	Manufacturer	Part Number
2x2 RCA Jacks (J5)	SWITCHCRAFT	PJRAS2X2S01
3x2 RCA Jacks (J4)	SWITCHCRAFT	PJRAS3X2S01
Mating Connector		
Two channel RCA interconnect cable	Monster Cable	BI100-1M

Video (J8)

Part Description	Manufacturer	Part Number
3x2 RCA Jacks (J4)	SWITCHCRAFT	PJRAS3X2S01

Power (J9)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board. The power connector supplies DC power to the board. The following table shows the power connector pinout.

Part Description	Manufacturer	Part Number
2.5 mm Power Jack (J9)	SWITCHCRAFT	RAPC712
	Digi-Key	SC1152-ND
Mating Power Supply (shipped with EZ-KIT Lite)		
7.5V Power Supply	GlobTek	TR9CC2000LCP-Y

The power connector supplies DC power to the EZ-KIT Lite board. Table 2-9 shows the power supply specifications.

Table 2-9. Power Supply Specification

Terminal	Connection
Center pin	+7.5 VDC@2amps
Outer Ring	GND

FlashLINK (P1)

The FlashLINK connector allows you to configure and program the STMicroelectronics DSM2150 flash/PLD chip. See "Configuring Flash Memory" on page 1-12 for more information about the FlashLINK connector.

Part Description	Manufacturer	Part Number
Right-angle 7X2 Shrouded 0.1 spacing (J10)	TYCO	2-767004-2
Mating Assembly		
FlashLINK JTAG Programmer	ST Micro	FL-101B

RS232 (P2)

The RS232-compatible connector is described in Table 2-10.

Table 2-10. RS232 Connector

Part Description	Manufacturer	Part Number
DB9, Male, Right Angle (P2)	Digi-Key	A2096-ND
Mating Assembly		
2m Female to female cable	Digi-Key	AE1016-ND

SPORT0 (P3)

The SPORT0 connector is linked to a 20-pin connector. The connector's pinout can be found in "Schematics" on page B-1. For pricing and availability on these connectors, contact AMP.

Part Description	Manufacturer	Part Number
20 position AMPMODU system 50 receptacle (P3)	AMP	104069-1
Mating Connectors		
20 position ribbon cable connector	AMP	111196-4
20 position AMPMODU system 20 connector	AMP	2-487937-0
20 position AMPMODU system 20 connector (w/o lock)	AMP	2-487938-0
Flexible film contacts (20 per connector)	AMP	487547-1

JTAG (P4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. When an emulator is connected to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

A BILL OF MATERIALS

The bill of materials corresponds to the board schematics on page B-1. Please check the latest schematics on the Analog Devices website, http://www.analog.com/Processors/Processors/DevelopmentTools/technicalLibrary/manuals/DevToolsIndex.html#Evaluation%20Kit%20Manuals.

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
1	2	74LVC14A SOIC14 HEX-INVER-SCHMITT-TRIGGER	U10,U41	TI	74LVC14AD
2	1	IDT74FCT3244APY SSOP20 3.3V-OCTAL-BUFFER	U31	IDT	IDT74FCT3244APY
3	1	IDT74FCT3807AQ QSOP20 3.3V 1-10 CLOCK DRIVER	U4	IDT	IDT74FCT3807AQ
4	1	CY7C64603-128 PQFP128 USB-TX/RXMICROCONTROLLER	U34	CYPRESS	CY7C64603-128NC
5	1	MMBT4401 SOT-23 NPN TRANSISTOR 200MA	Q1	FAIRCHILD	MMBT4401
6	1	74LVC00AD SOIC14	U9	PHILIPS	74LVC00AD
7	1	CY7C1019BV33-15VC SOJ32 128K X 8 SRAM	U39	CYPRESS	CY7C1019BV33-12VC
8	1	SN74AHC1G02 SOT23-5 SINGLE-2 INPUT-NOR	U44	TI	SN74AHC1G02DBVR
9	1	SN74LV164A SOIC14 8-BIT-PARALLEL-SERIAL	U35	TI	SN74LV164AD
10	1	CY7C4201V-15AC TQFP3264-BYTE-FIFO	U43	CYPRESS	CY7C4201V-15AC
11	1	12.0MHZ THR OSC006 CRYSTAL	Y1	DIG01	300-6027-ND
12	1	SN74AHC1G00 SOT23-5 SINGLE-2-INPUT-NAND	U42	TI	SN74AHC1G00DBVR
13	1	12.288MHZ SMT OSC003	U11	DIG01	SG-8002CA-PCC-ND

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
14	1	SN74LVC1G125 SOT23-5 SINGLE-3STATE-BUFFER	U7	TI	SN74LVC1G125DBVR
15	1	FDS9431A PMOSFET	U32	FAIRCHILD SEMI	FDS9431A
16	1	MT48LC32M16A2TG-75 TSOP54 512MB -SDRAM	U8	MICRON	MT48LC16M16A2TG-75
17	1	27MHZ SMT OSC003	U3	EPSON	SG-8002CA MP
18	1	32.768KHZ SMT OSC008	U2	EPSON	MC-156 32.768KA-A2
19	2	PSD4256G6V-10UI TSOP54 1MB-FLASH/GPIO	U5–6	ST MICRO	PSD4256G6V-10UI
20	1	IDT2305-1DC SOIC8 1 TO 5 ZERO DELAY CLK BUF	U46	INTEGRATED SYS	ICS9112AM-16
21	1	SN74LVC1G32 SOT23-5 SINGLE-2 INPUT OR GATE	U21	TI	SN74LVC1G32DBVR
22	1	BF533 24LC00-SN "U33" SEE 1000127	U33	ANALOG DEVICES	
23	2	1000pF 50V 5% 1206 CERM	C96–97	AVX	12065A102JAT2A
24	6	2200pF 50V 5% 1206 NPO	C12,C17,C22, C27,C32,C37	AVX	12065A222JAT050
25	1	ADM708SAR SOIC8 VOLTAGE-SUPERVISOR	U29	ANALOG DEVICES	ADM708SAR
26	1	ADP3338AKC-33 SOT-223 3.3V-1.0AMP REGULATOR	VR1	ANALOG DEVICES	ADP3338AKC-3.3

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
27	1	ADP3339AKC-5 SOT-223 5V-1.5A REGULATOR	VR5	ANALOG DEVICES	ADP3339AKC-5-REEL
28	2	ADP3339AKC-33 SOT-223 3.3V 1.5A REGULATOR	VR3–4	ANALOG DEVICES	ADP3339AKC-3.3-RL
29	1	ADP3336ARM MSOP8 ADJ 500MA REGULATOR	VR6	ANALOG DEVICES	ADP3336ARM-REEL
30	1	ADV7171KSU TQFP44 VID-ENCODER	U27	ANALOG DEVICES	ADV7171KSU
31	1	10MA AD1580BRT SOT23D 1.2V-SHUNT-REF	D1	ANALOG DEVICES	AD1580BRT
32	2	ADG752BRT SOT23-6 CMOS-SPDT-SWITCH	U25–26	ANALOG DEVICES	ADG752BRT
33	3	AD8061ART SOT23-5 300MHZ-AMP	U22–24	ANALOG DEVICES	AD8061ART-REEL
34	1	ADM3202ARN SOIC16 RS232-TXRX	U30	ANALOG DEVICES	ADM3202ARN
35	1	ADV7183KST LQFP80 VID-DECODER	U28	ANALOG DEVICES	ADV7183KST
36	8	AD8606AR SOIC8 OPAMP	U12–13,U15–20	ANALOG DEVICES	AD8606AR
37	1	ADSP-BF533SKBC MINIBGA160	U1	ANALOG DEVICES	
38	1	AD1836AAS MQFP52 MULTI-CHAN- NEL-96KHZ-CODEC	U14	ANALOG DEVICES	AD1836AAS

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
39	5	RUBBER FEET BLACK	MH1–5	MOUSER	517-SJ-5018BK
40	1	PWR 2.5MM_JACK CON005 RA	J9	SWITCHCRAFT	SC1152-ND12
41	1	USB 4PIN CON009 USB	J10	MILL-MAX	897-30-004-90-000000
42	1	RCA 2X2 CON013	J5	SWITCHCRAFT	PJRAS2X2S01
43	1	.05 10X2 CON014 RA	P3	AMP	104069-1
44	5	SPST-MOMENTARY SWT013 6MM	SW4-8	PANASONIC	EVQ-PAD04M
45	1	IDC 7X2 IDC7X2SRDRA RIGHT ANGLE SHROUDED	P1	MOLEX	70247-1401
46	3	0.05 45X2 CON019 SMT SOCKET	J1–3	SAMTEC	SFC-145-T2-F-D-A
47	4	DIP6 SWT017	SW1–3,SW9	DIG01	CKN1364-ND
48	2	RCA 3X2 CON024 RA	J4,J8	SWITCHCRAFT	PJRAS3X2S01
49	14	0.00 1/8W 5% 1206	R27–30,R148, R157–158,R167, R174–175, R177–178, R182,R193	YAGEO	0.0ECT-ND
50	7	AMBER-SMT LED001 GULL-WING	LED4–9, LED11	PANASONIC	LN1461C-TR

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
51	12	330pF 50V 5% 805 NPO	C13,C18,C23, C28,C33,C38	AVX	08055A331JAT
52	42	0.01uF 100V 10% 805 CERM	C4,C85,C87, C108,C112–113, C123–124, C126–128, C136,C146–147, C149–155, C159–161	AVX	08051C103KAT2A
53	8	0.22uF 25V 10% 805 CERM	C129–130, C137–142	AVX	08053C224FAT
54	73	0.1uF 50V 10% 805 CERM	C6,C8,C71–72, C75–81,C84, C86,C88–95, C98–101,C105, C109–111, C114–122,C125, C131	AVX	08055C104KAT
55	8	0.001uF 50V 5% 805 NPO	C7,C9–11, C49–50,C52–53	AVX	08055A102JAT2A
56	8	10uF 16V 10% C TANT	CT13, CT21–27	SPRAGUE	293D106X9016C2T
57	45	10K 100MW 5% 805	R1, R4, R10, R12–13,R15–16	AVX	CR21-103J-T
58	9	33 100MW 5% 805	R5–6, R8–9,R31, R144,R179,R183	AVX	CR21-330JTR
59	2	4.7K 100MW 5% 805	R17,R220	AVX	CR21-4701F-T

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
60	1	1M 100MW 5% 805	R202	AVX	CR21-1004F-T
61	1	1.5K 100MW 5% 805	R203	AVX	CR21-1501F-T
62	1	1.2K 1/8W 5% 1206	R129	DALE	CRCW1206-122JRT1
63	6	49.9K 1/8W 1% 1206	R38,R45,R54, R62,R70,R78	AVX	CR32-4992F-T
64	2	2.21K 1/8W 1% 1206	R212–213	AVX	CR32-2211F-T
65	1	2000pF 50V 5% 1206 CERM	C83	AVX	12065A202JAT2A
66	12	100pF 100V 5% 1206 NPO	C15,C20,C25, C30,C35,C40,	AVX	12061A101JAT2A
67	5	10uF 16V 10% B TANT	CT1–2,CT14–16	AVX	TAJB106K016R
68	4	100 100MW 5% 805	R149,R152, R154–155	AVX	CR21-101J-T
69	6	220pf 50V 10% 1206 NPO	C16,C21,C26, C31,C36,C41	AVX	12061A221JAT2A
70	4	600 100MHZ 200MA 603 0.50 BEAD	FER14–17	MURATA	BLM11A601SPT
71	3	2A S2A_RECT DO-214AA SILICON RECTIFIER	D2–4	GENERALSEMI	S2A
72	12	600 100MHZ 500MA 1206 0.70 BEAD	FER1–5, FER9–11, FER18–19, FER18–19, FER21–22	DIGI-KEY	240-1019-1-ND

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
73	4	237 1/8W 1% 1206	R93,R95,R97, R99	AVX	CR32-2370F-T
74	4	750K 1/8W 1% 1206	R86,R90,R94, R96	DALE/VISHAY	CRCW12067503FRT1
75	16	5.76K 1/8W 1% 1206	R82–85,R87–89, R91–92,R98	PHYCOMP	9C12063A5761FKHFT
76	6	11.0K 1/8W 1% 1206	R34,R48,R50, R58,R66,R74	DALE	CRCW12061102FRT1
77	8	120PF 50V 5% 1206 NPO	C42–45,C55, C57–59	PHILLIPS	1206CG121J9B200
78	1	68PF 50V 5% 1206	C82	PHILLIPS	1206CG680J9B200
79	1	1UF 16V 10% 805 X7R	C5	MURATA	GRM40X7R105K016AL
80	12	75 1/8W 5% 1206	R113–114, R116–117, R120–121	PHILIPS	9C12063A75R0JLHFT
81	2	30PF 100V 5% 1206	C206–207	AVX	12061A300JAT2A
82	1	68UF 6.3V 20% D TANT	CT28	PANASONIC	ECS-TOJD686R
83	6	680PF 50V 1% 805 NPO	C14,C19,C24, C29,C34,C39	AVX	08055A681FAT2A
84	3	10UF 25V +80-20% 1210 Y5V	C198–200	MURATA	GRM235Y.5V106Z025

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
85	6	2.74K 1/8W 1% 1206	R41,R47,R57, R65,R73,R81	PANASONIC	ERJ-8ENF2741V
86	12	5.49K 1/8W 1% 1206	R35,R40,R42, R49,R51,R56, R59	PANASONIC	ERJ-8ENF5491V
87	6	3.32K 1/8W 1% 1206	R36,R43,R52, R60,R68,R76	DALE	CRCW12063321FRT1
88	6	1.65K 1/8W 1% 1206	R37,R44,R53, R61,R69,R77	PANASONIC	ERJ-8ENF1651V
89	10	10UF 16V 20% CAP002 ELEC	CT3–12	DIG01	PCE3062TR-ND
90	1	53.6K 1/10W 1% 805	R184	PHILIPS	9C08052A5362FKRT/R
91	1	10UH 47 +/-20 IND001	L12	DIG01	445-1202-2-ND
92	2	10K 50MW 5% BGA36	RN1–2	CTS	RT130B7
93	15	0.00 100MW 5% 805	R3,R22,R24–25, R111,R132, R135–136,R141, R186–189, R210,R222	VISHAY	CRCW0805 0.0 RT1
94	1	190 100MHZ 5A FER002	FER23	MURATA	DLW5BSN191SQ2
95	1	3.32K 100MW 1% 805	C188	DIG01	P3.32KCCTR-ND
96	3	22 1/10W 5% 805	R14, R180–181	VISHAY/DALE	CRCW0805220JRT1
97	6	0.68UH 0.72 10% 805	L4–9	MURATA	LQG21NR68K10T1

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
98	1	1A ZHCS1000 SOT23D SCHOTTKY	D5	ZETEX	ZHCS1000
99	1	5.6K 1/10W 5% 805	R140	VISHAY	CRCW0805562JRT1
100	3	2.2UH 0.63 10% 805	L1–3	MURATA	LQG21N2R2K10
101	3	1UF 10V 10% 805	C60–61,C104	AVX	0805ZC105KAT2A
102	2	18PF 50VDC 5% 805 CERM	C1, C3	PANASONIC	ECJ-2VC1H180J
103	1	10M 1/8W 5% 805	R20	AVX	CR21-106J-T
104	1	DB9 9PIN DB9M RIGHT ANGLE MALE	P2	3M	787203-2
105	7	1K 1/8W 5% 1206	R115,R118–119, R125–126,R131	AVX	CR32-102J-T
106	3	100K 1/8W 5% 1206	R112,R130,R176	CR1206-1003FRT 1	
107	2	22 1/8W 5% 1206	R200,R207	DALE	CRCW1206220JRT1
108	9	270 1/8W 5% 1206	R146–147, R160–162, R164–165,R168, R195	AVX	CR32-271J-T
109	1	680 1/8W 5% 1206	R163	AVX	CR32-681J-T
110	1	150 1/8W 1% 1206	R122	PANASONIC	ERJ-8ENF1500V
111	2	RED-SMT LED001 GULL-WING	LED2–3	PANASONIC	LN1261C

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
112	1	GREEN-SMT LED001 GULL-WING	LED1	PANASONIC	LN1361C
113	6	604 1/8W 1% 1206	R39,R46,R55, R63,R71,R79	PANASONIC	ERJ-8ENF6040V
114	4	1uF 25V 20% A TANT -55+125	CT17–20	PANASONIC	ECS-T1EY105R
115	2	ADG774A QSOP16 QUICKSWITCH-257	U37–38	ANALOG DEVICES	ADG774ABRQ
116	1	IDC 7X2 IDC7X2 HEADER	P4	BERG	54102-T08-07
117	1	2.5A RESETABLE FUS001	F1	RAYCHEM CORP.	SMD250-2

ADSP-BF533 EZ-KIT Lite

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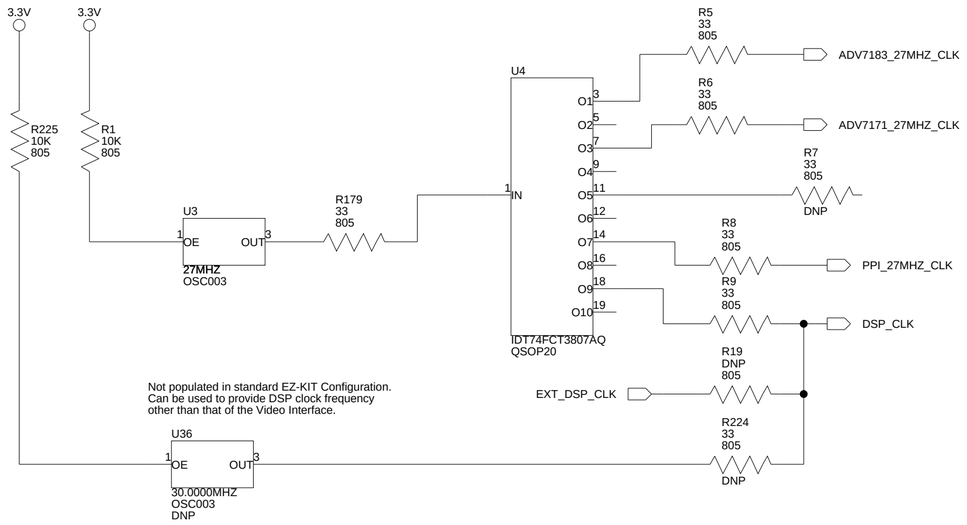
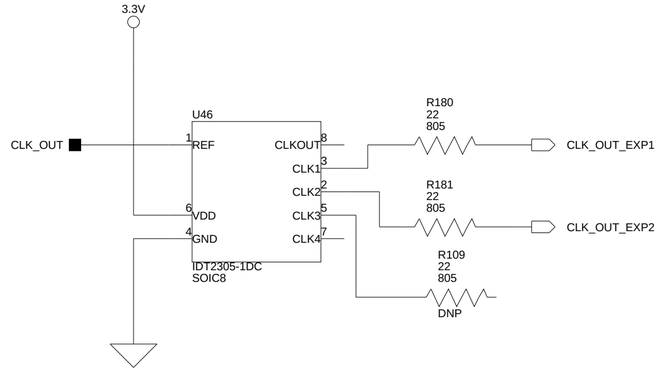
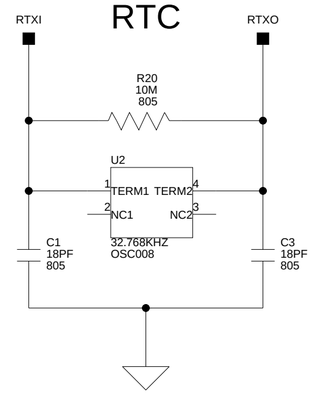
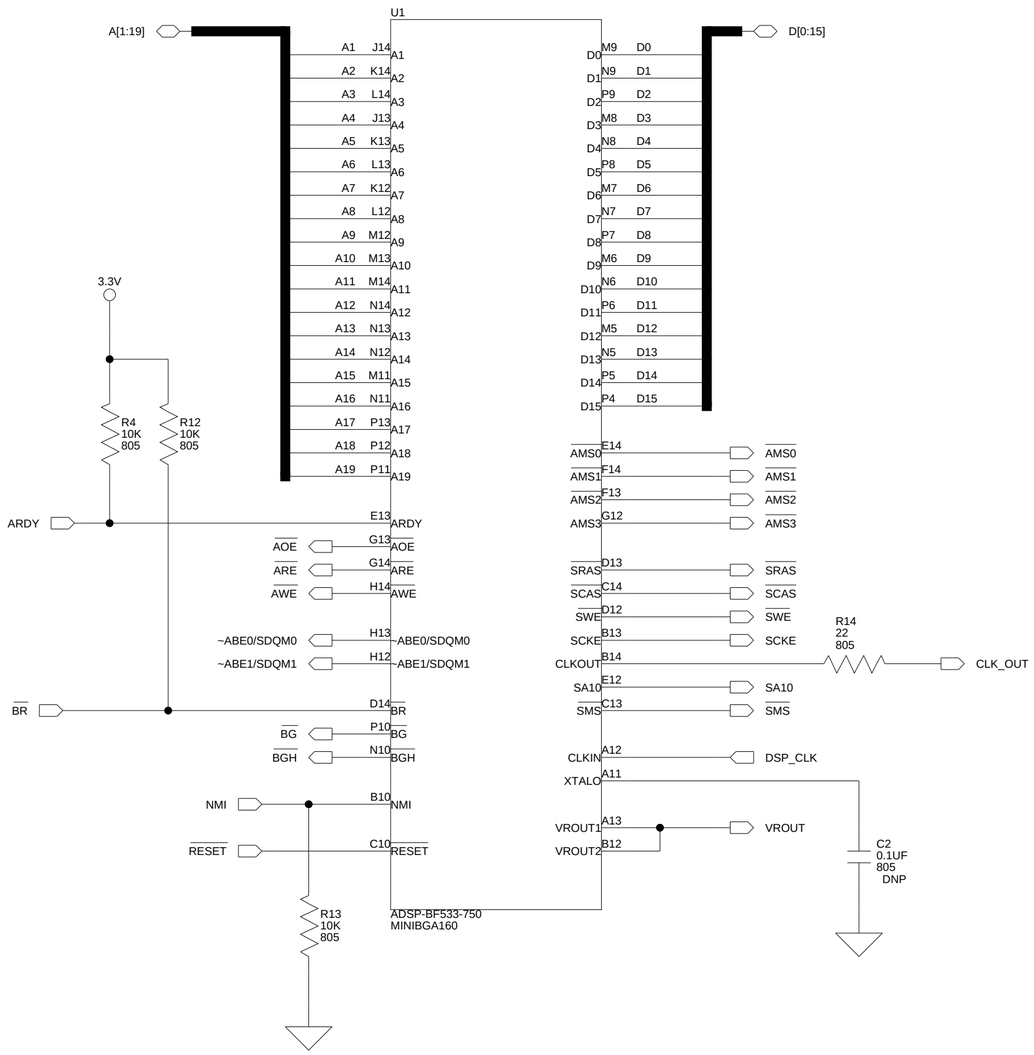
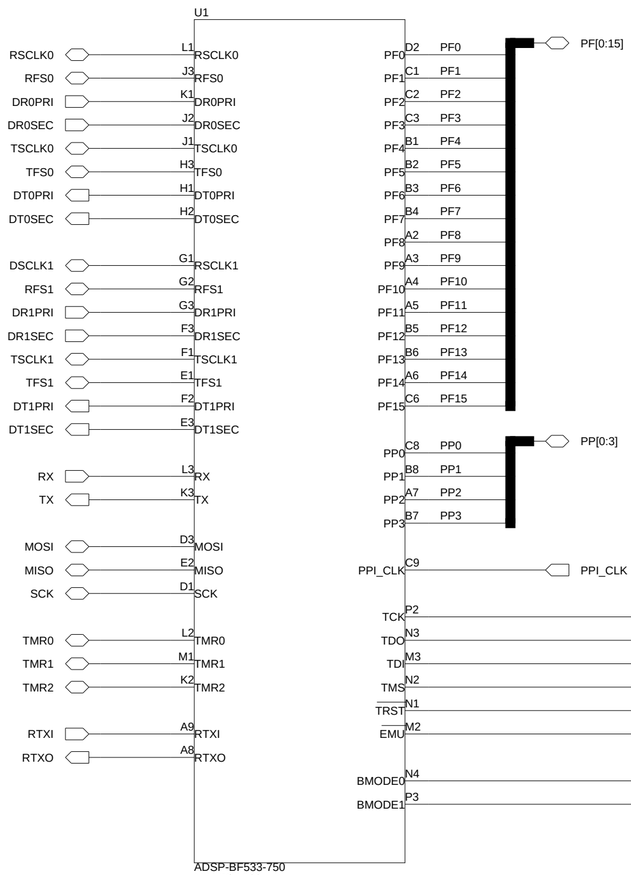
Size C	Board No. A0167-2001		Rev 1.6C
Date 12-21-2004_15:13		Sheet 1 of 12	

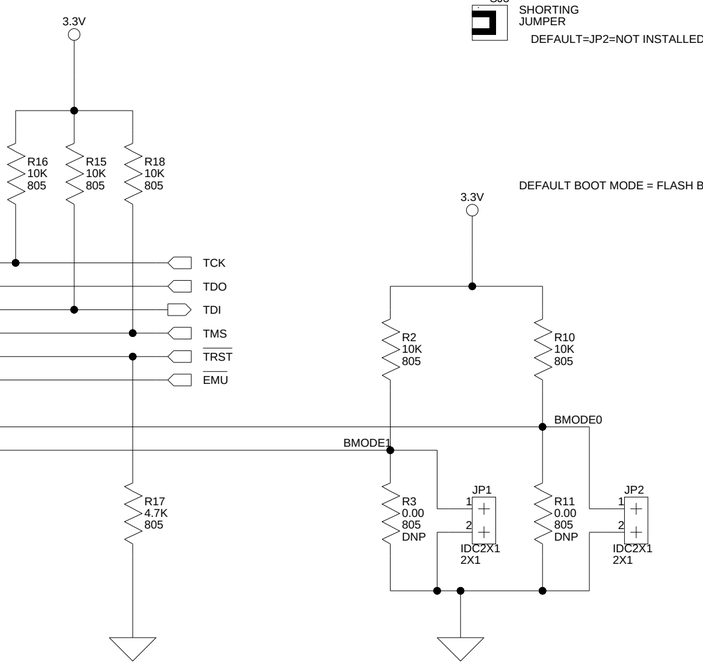


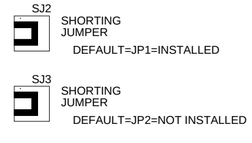












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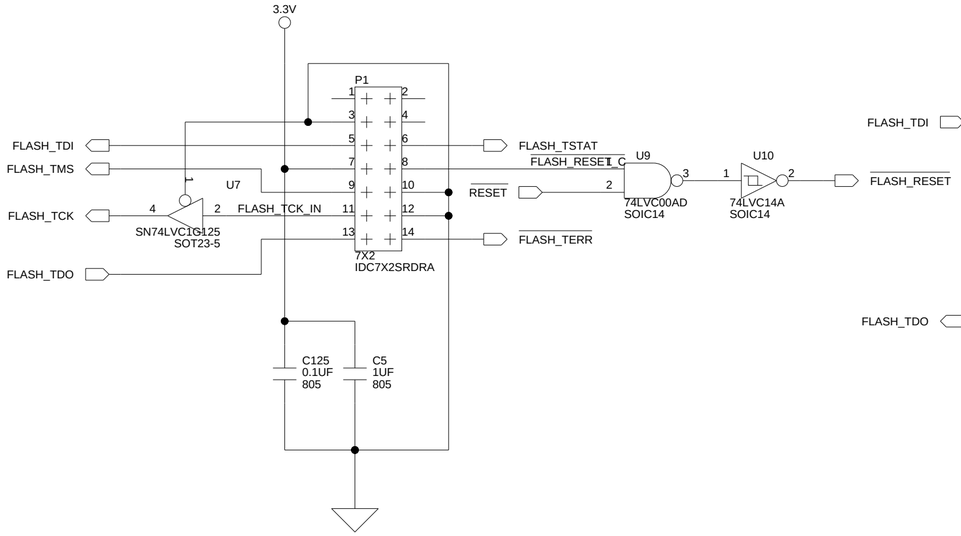
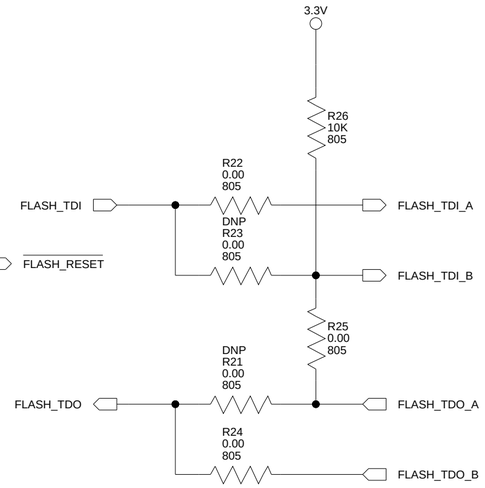
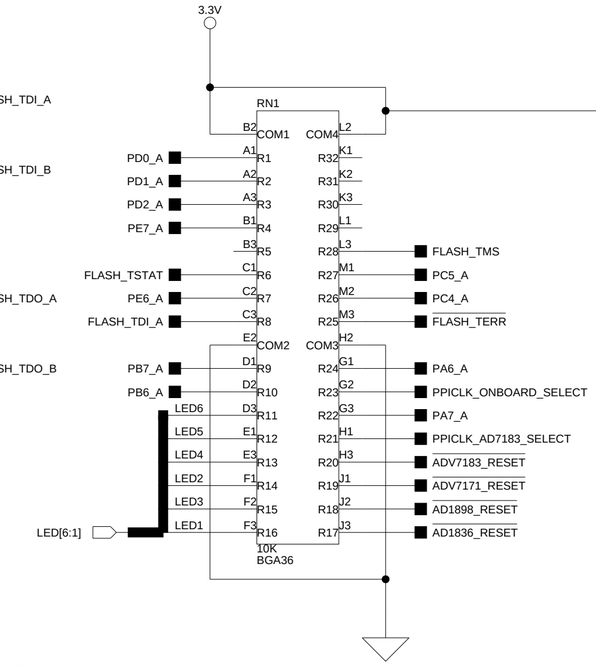
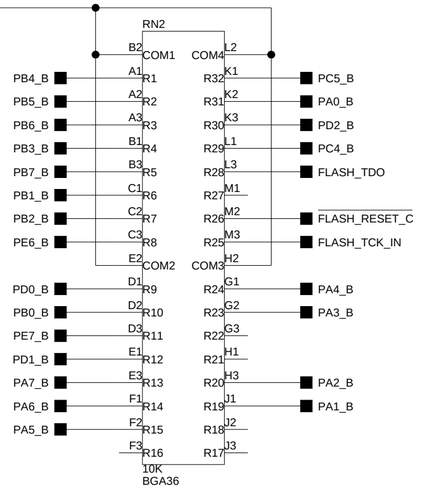
FlashLINK JTAG HEADER





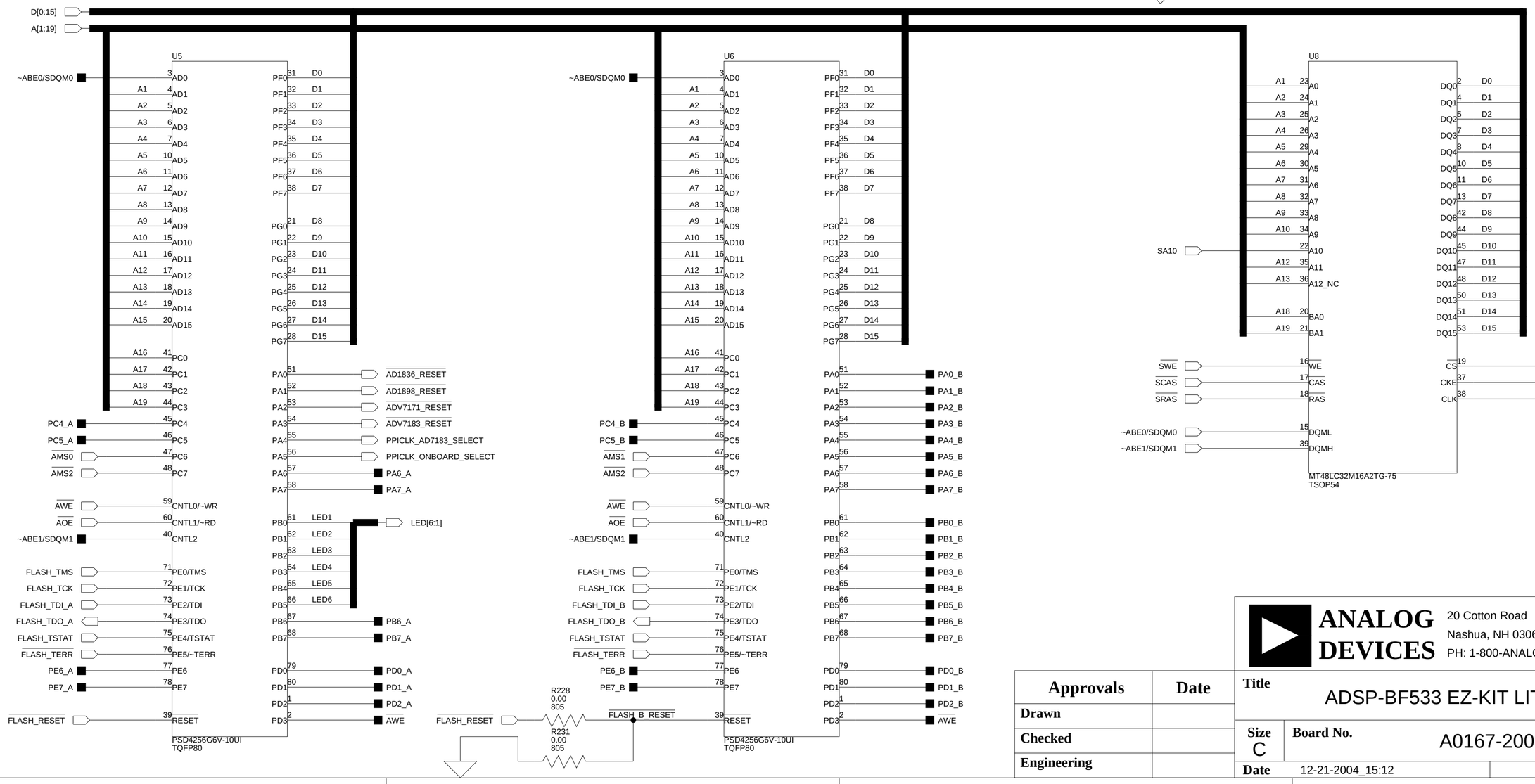




FLASH A (1MB)
512K x 16

FLASH B (1MB)
512K x 16

SDRAM 512Mb
(64MB - 32M x 16)



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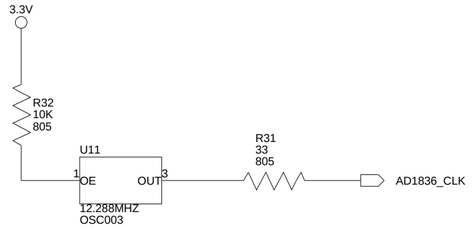

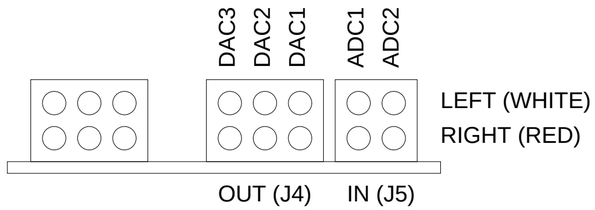

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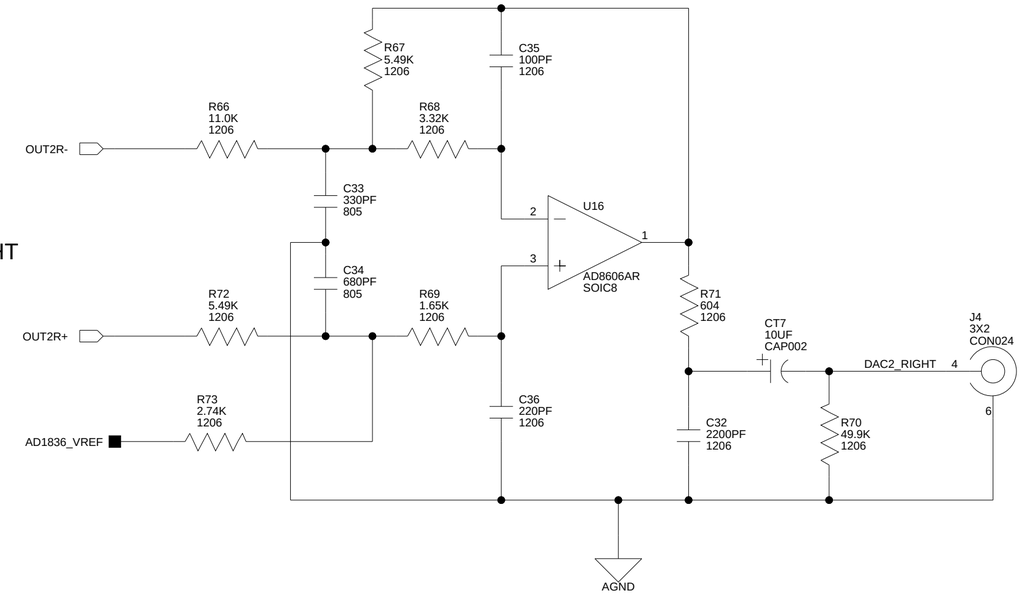
Title	ADSP-BF533 EZ-KIT LITE - AUDIO CODEC	
Size C	Board No. A0167-2001	Rev 1.6C
Date 12-21-2004_15:12	Sheet 4 of 12	

DAC2 RIGHT



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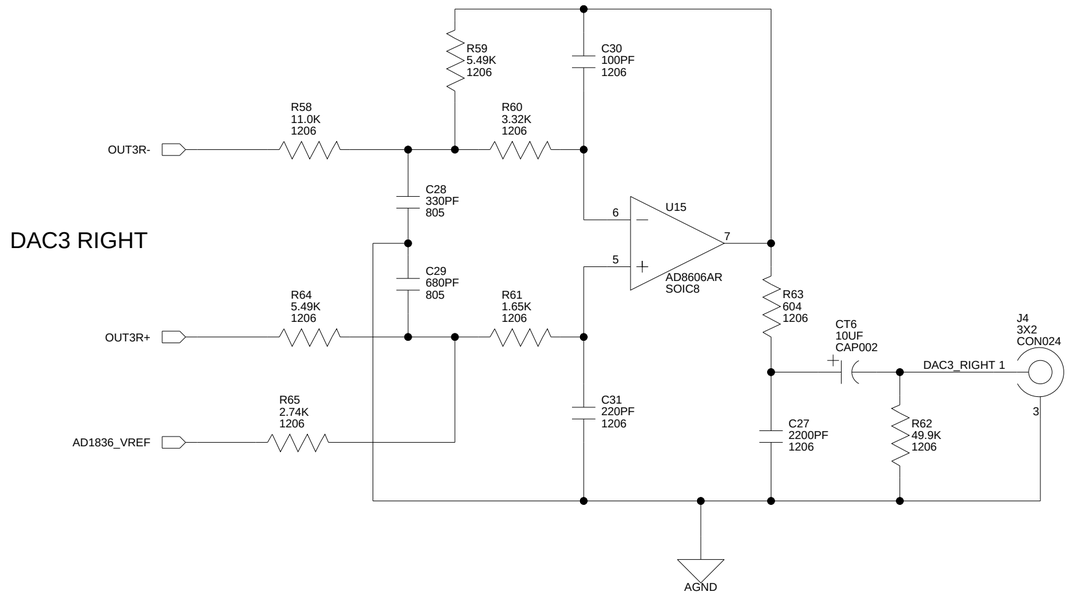

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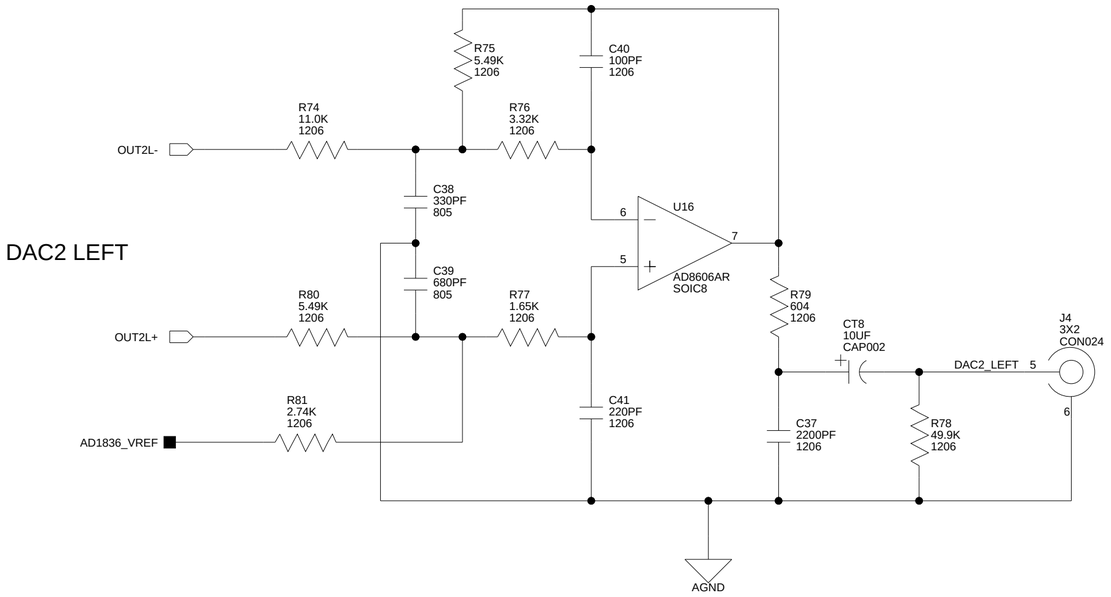

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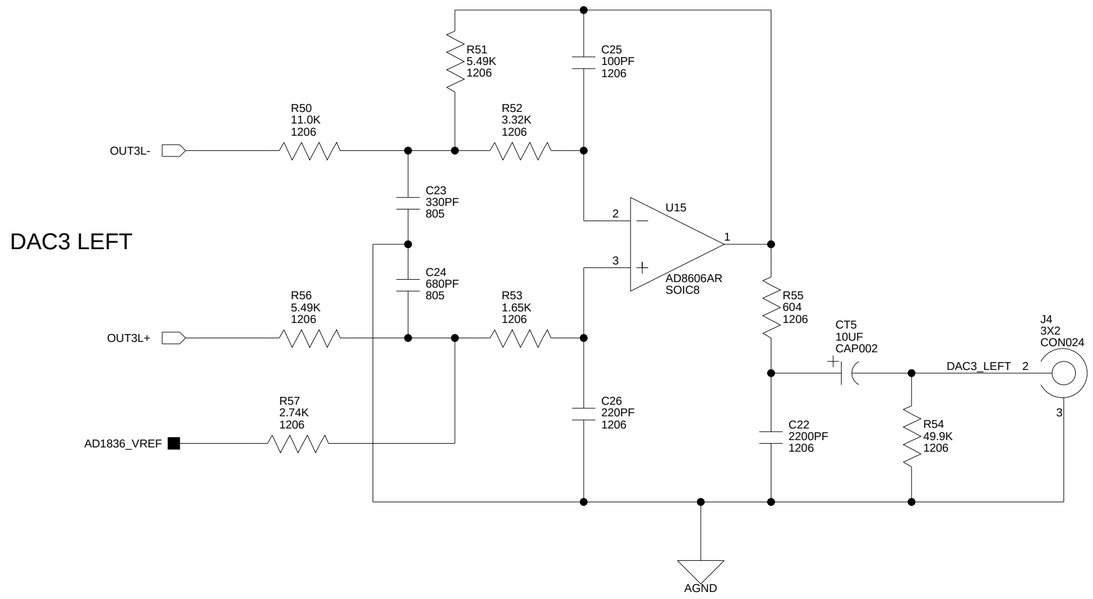

DNP = Do Not Populate

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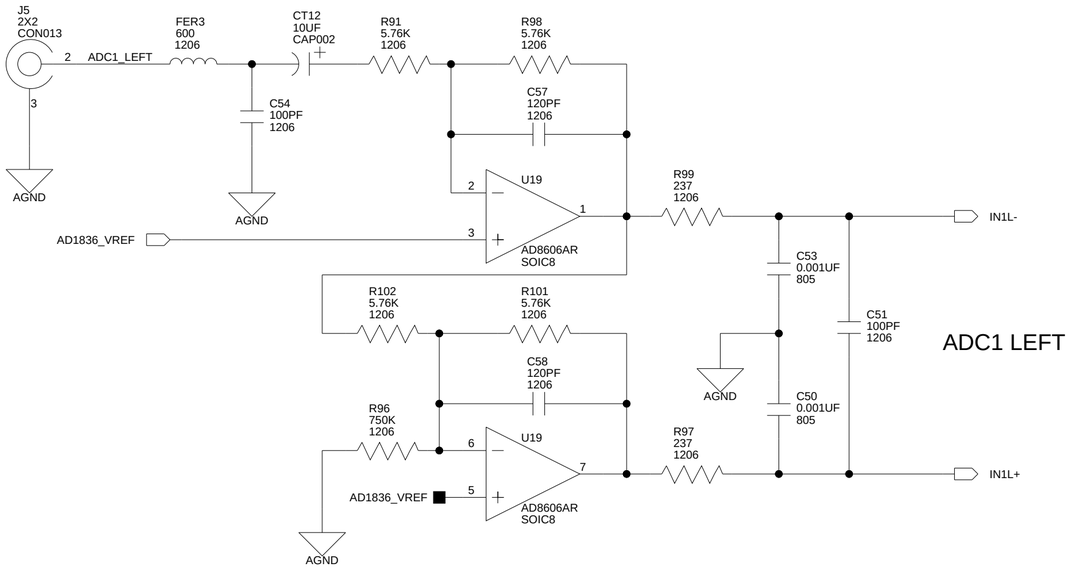
Title ADSP-BF533 EZ-KIT LITE - AUDIO OUT

Size	Board No.	Rev
C	A0167-2001	1.6C

Date	12-21-2004_15:12	Sheet	5	of	12



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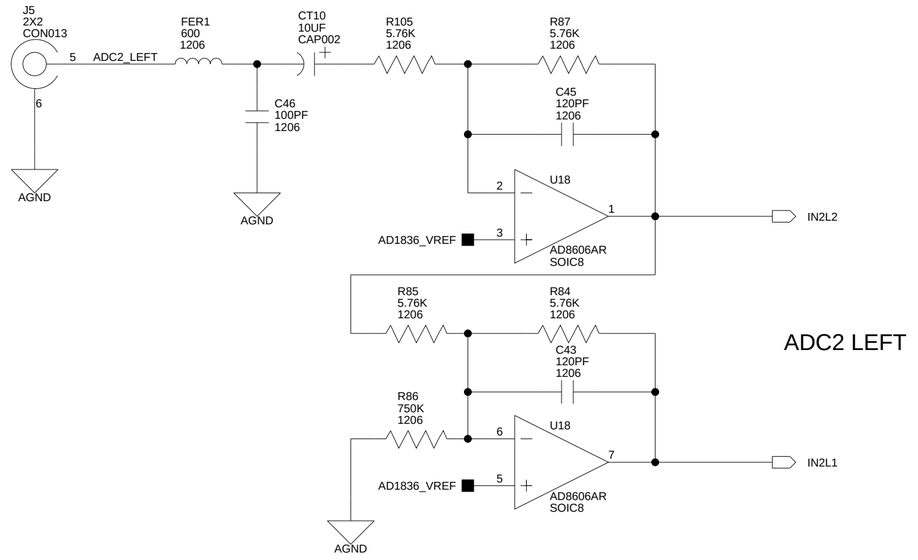

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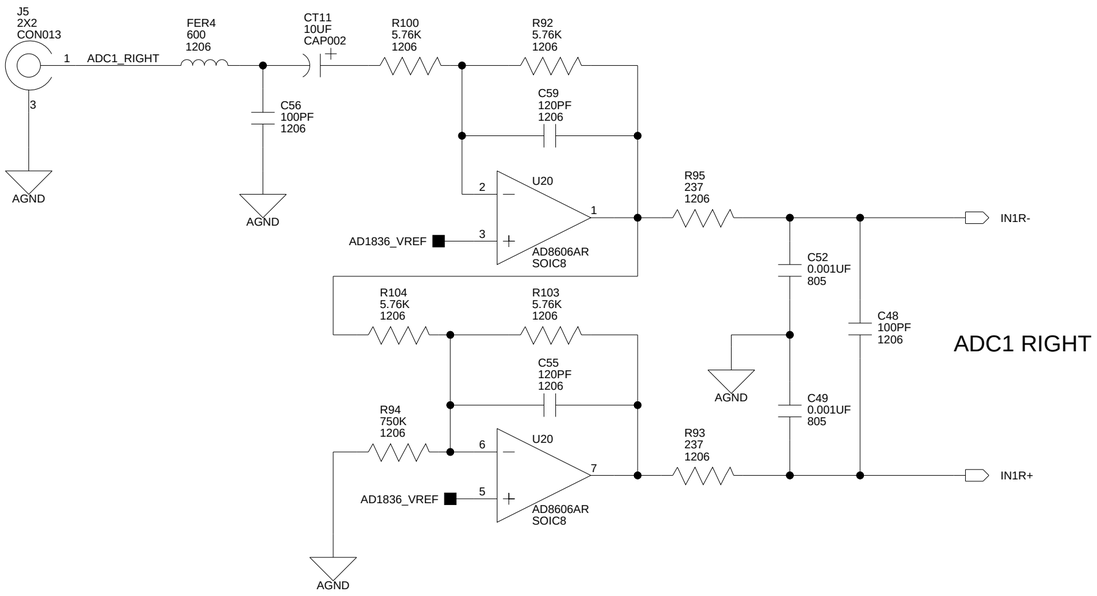

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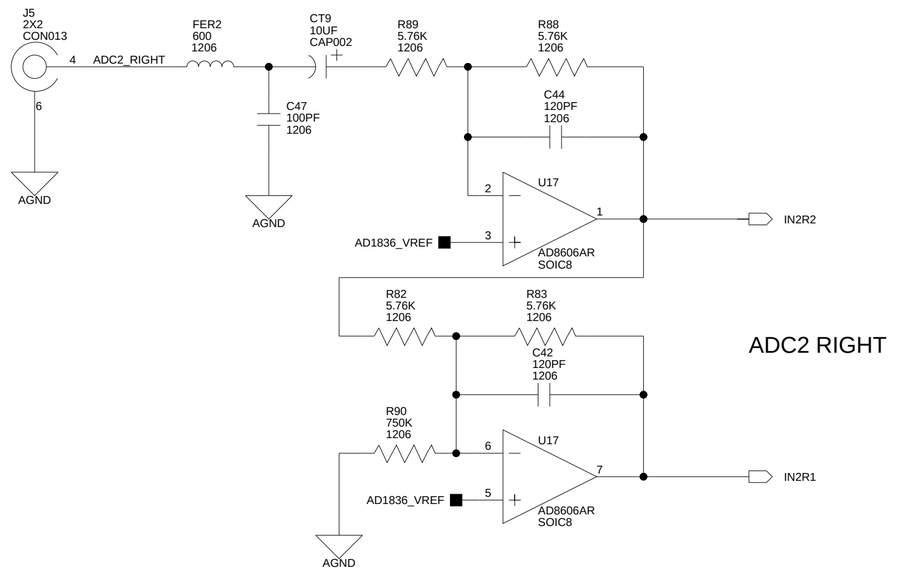

ADC2 RIGHT

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Title: ADSP-BF533 EZ-KIT LITE - AUDIO IN

Size	Board No.	Rev
C	A0167-2001	1.6C

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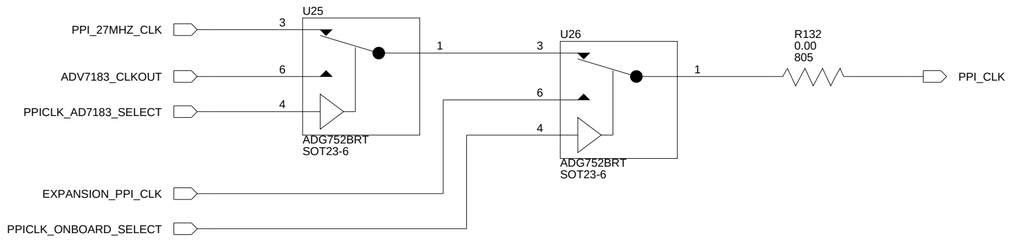
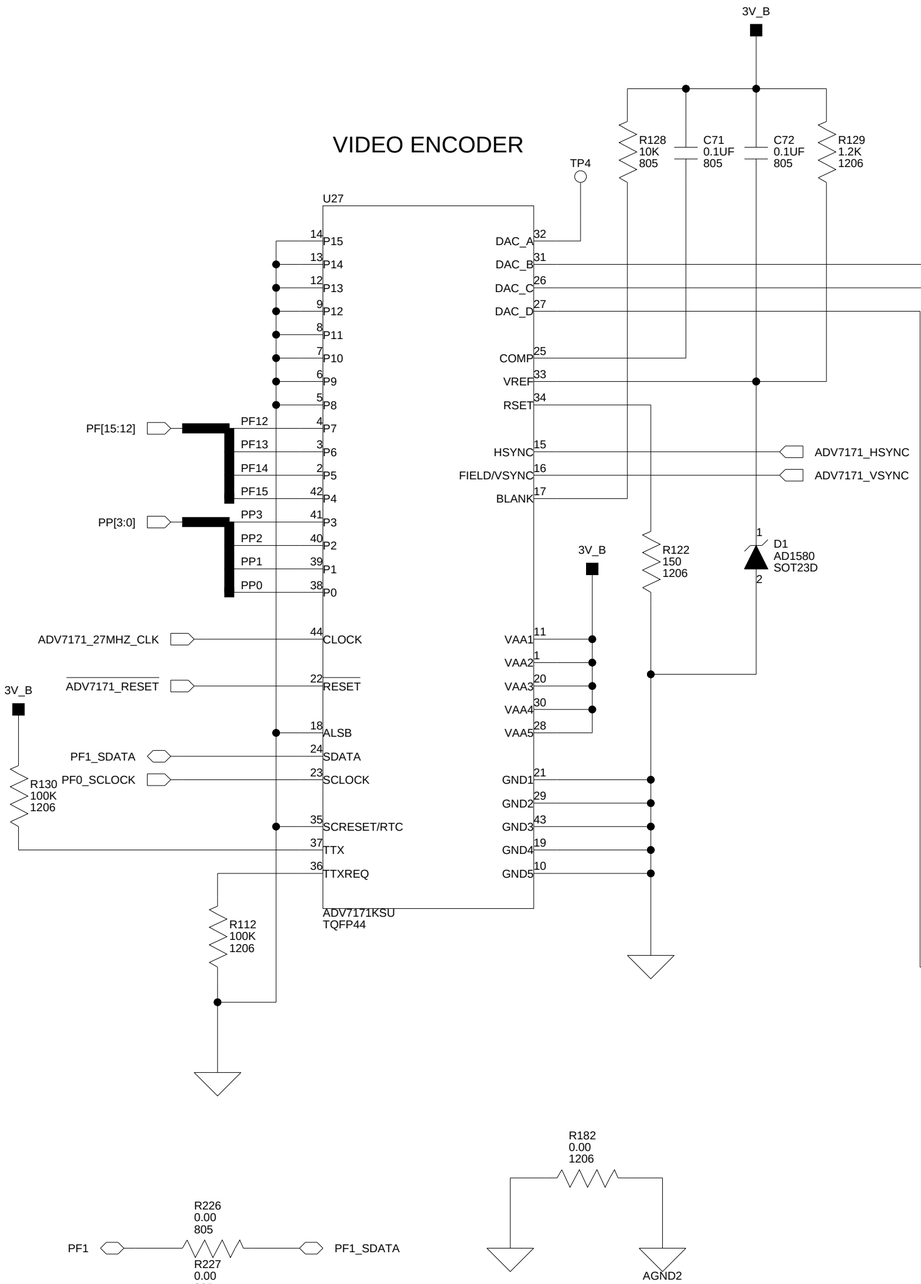
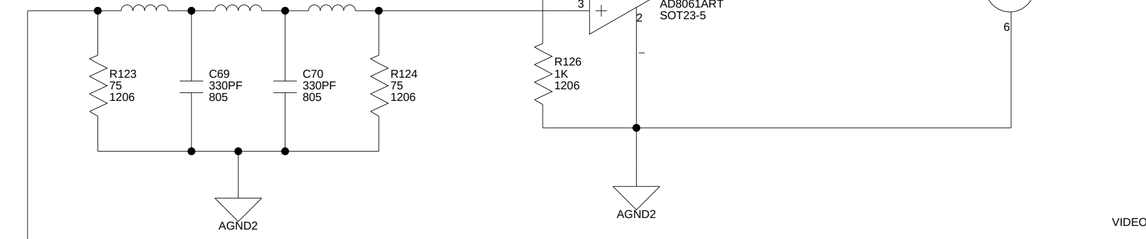
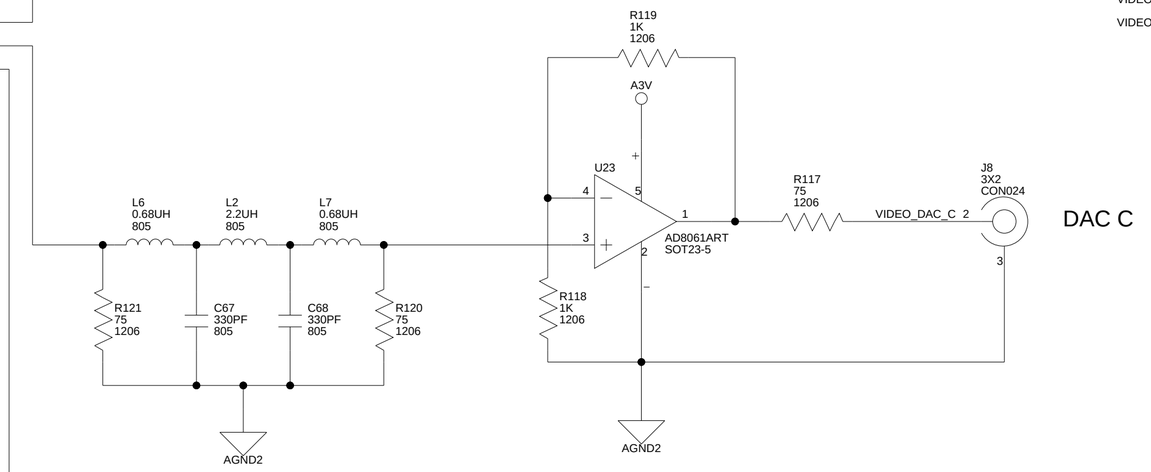
PPICLK_ONBOARD_SELECT	PPICLK_AD7183_SELECT	PPCLK
0	0	PPI_27MHZ_CLK (DEFAULT)
0	1	ADV7183_CLKOUT
1	X	EXPANSION_CLK

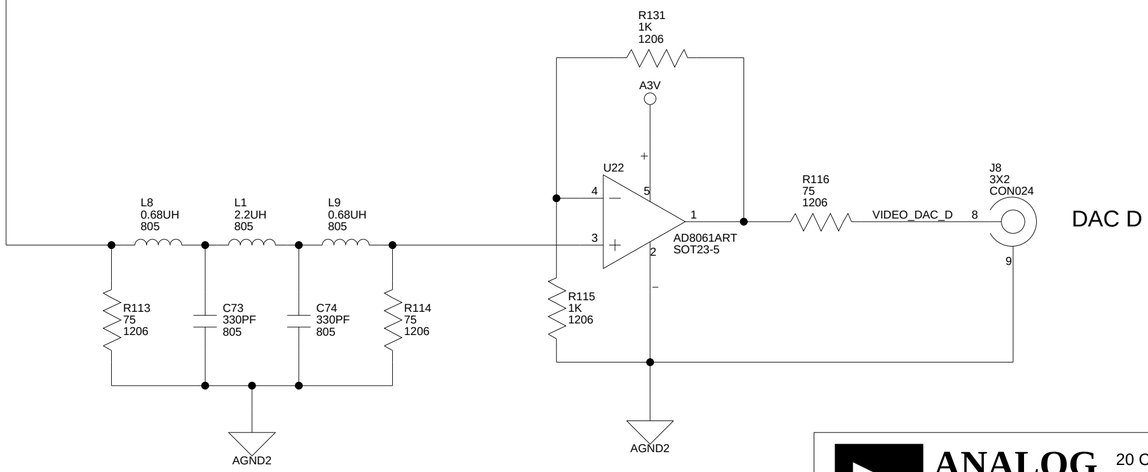
	DAC B	DAC C	DAC D
Composite Video	CVSB		CVSB
Component Video	B	R	G
Differential Component Video	U	V	Y
S Video		C	Y

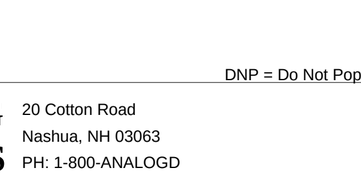












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Title: ADSP-BF533 EZ-KIT LITE - VIDEO OUT

Size	Board No.	Rev
C	A0167-2001	1.6C

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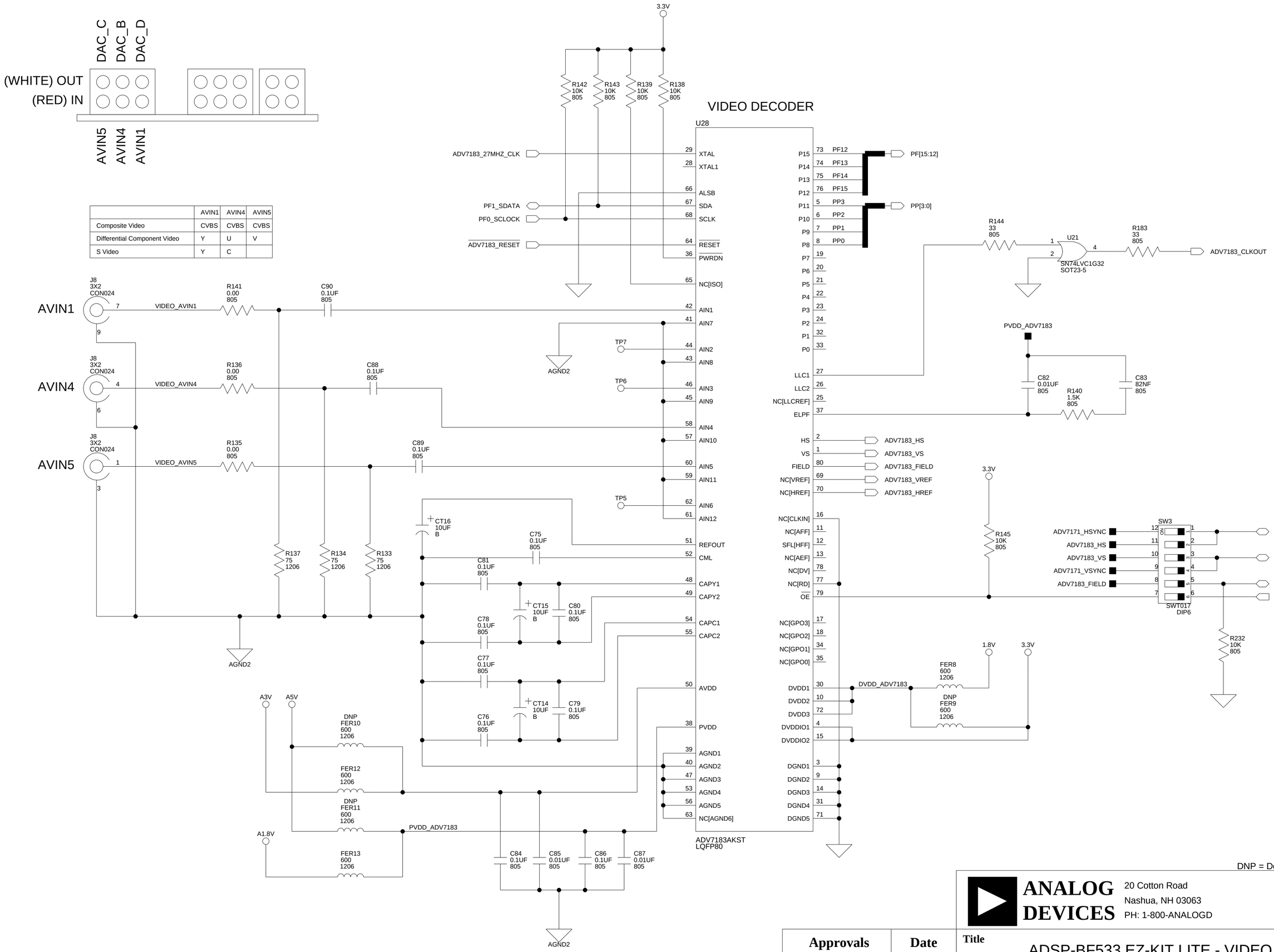

	AVIN1	AVIN4	AVIN5
Composite Video	CVBS	CVBS	CVBS
Differential Component Video	Y	U	V
S Video	Y	C	

DNP = Do Not Populate

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Title: ADSP-BF533 EZ-KIT LITE - VIDEO IN

Size	Board No.	Rev
C	A0167-2001	1.6C

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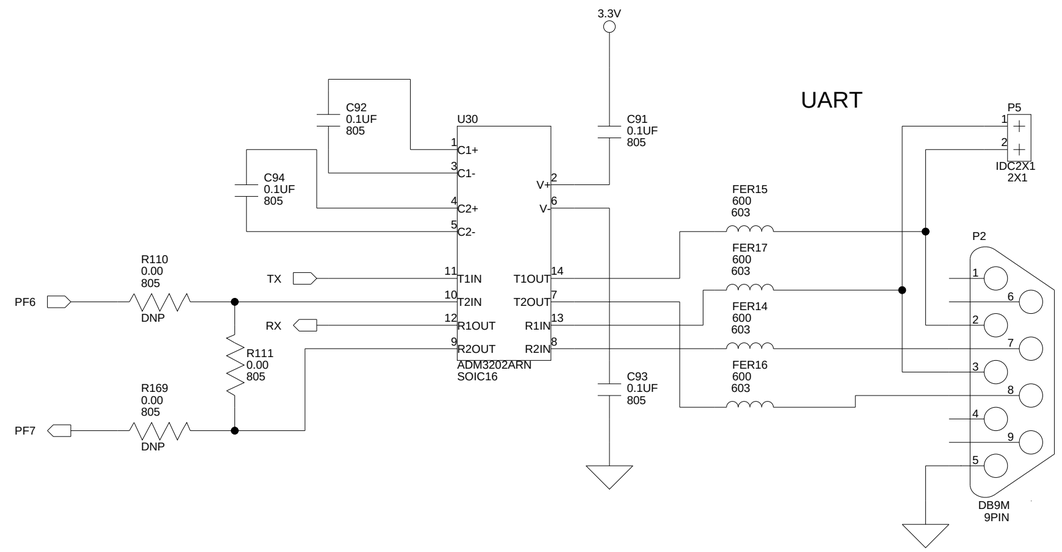

SW8 PB Enable Switch

Position	Function
1-4	Connects the push buttons to the Programmable Flags of the DSP Useful if using the PFs for another purpose.
5,6	Connects SPORT0 frame sync and clock together external to the DSP Required when AD1836 is in I2S mode

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Title: ADSP-BF533 EZ-KIT IO/RESET/UART

Size	Board No.	Rev
C	A0167-2001	1.6C

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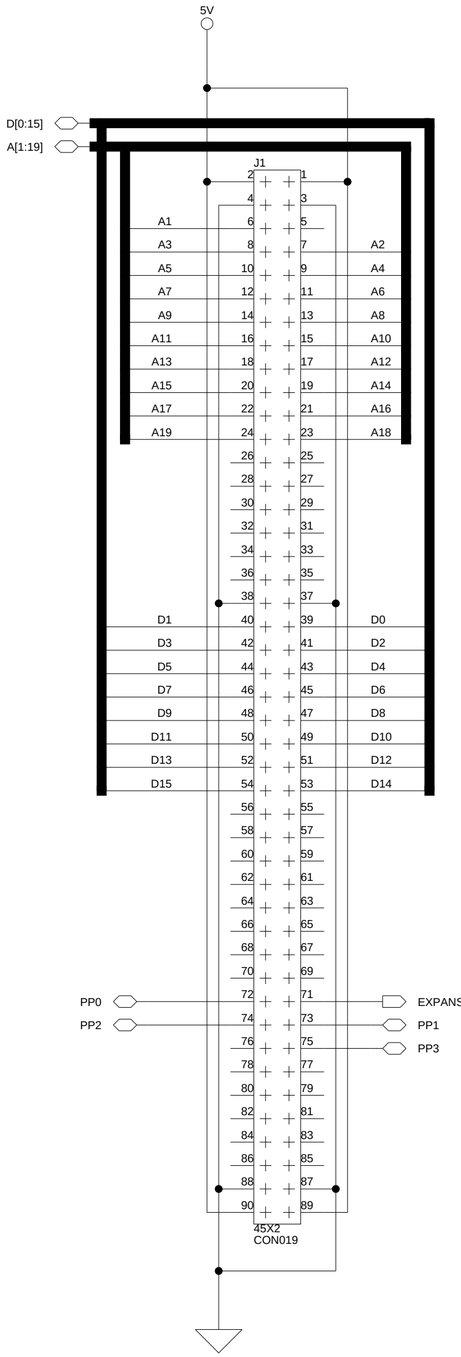
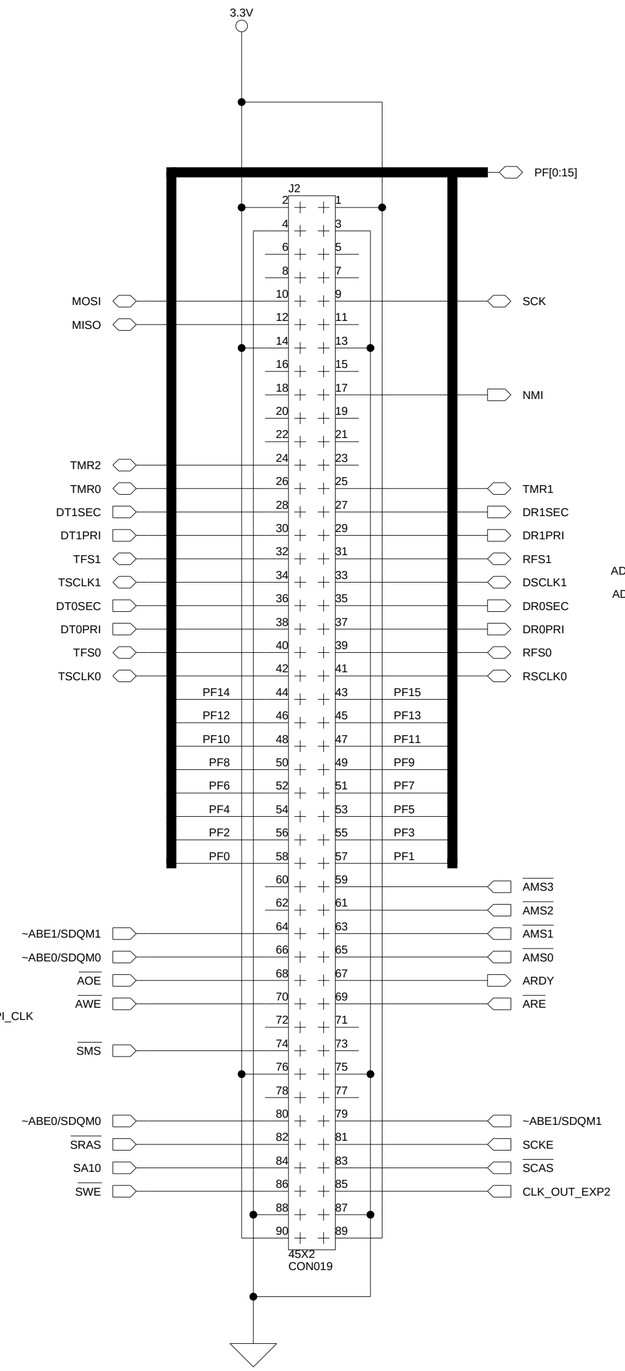
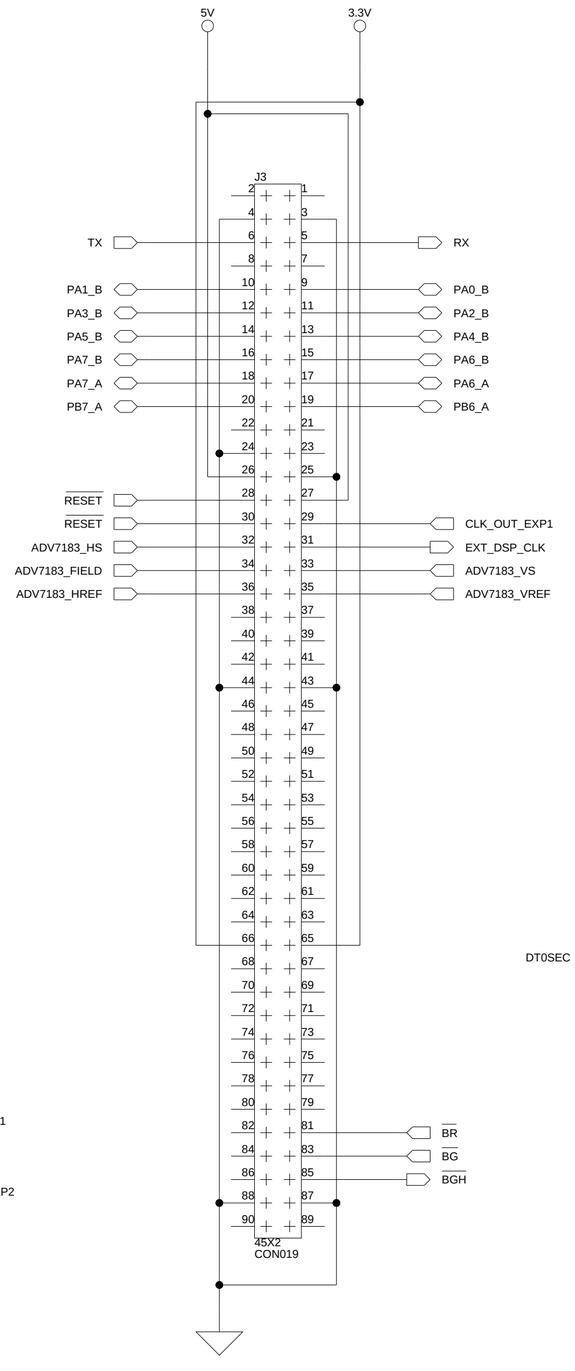
EXPANSION INTERFACE (TYPE B)

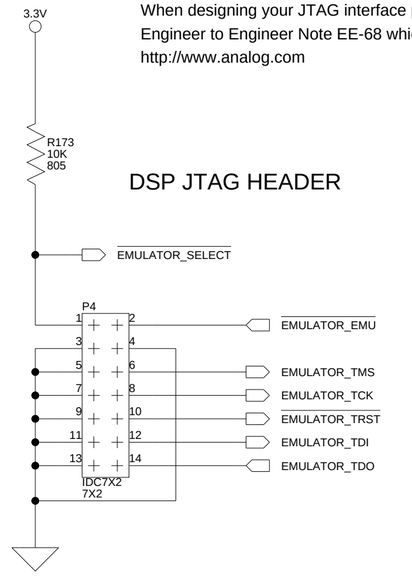


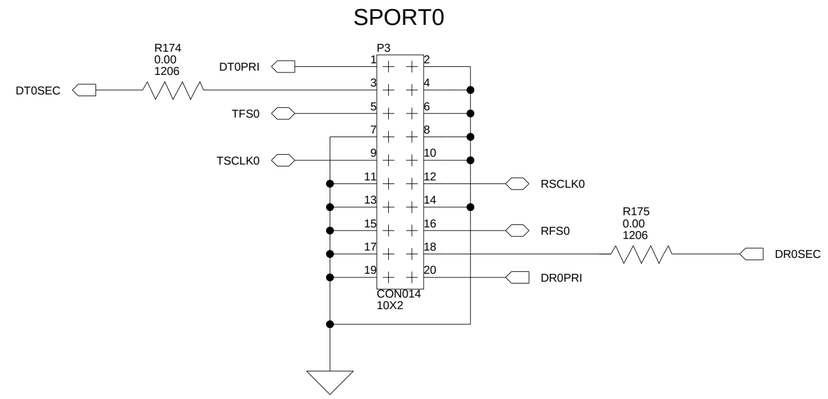




All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com





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Title: ADSP-BF533 EZ-KIT LITE - CONNECTOR

Size	Board No.	Rev
C	A0167-2001	1.6C

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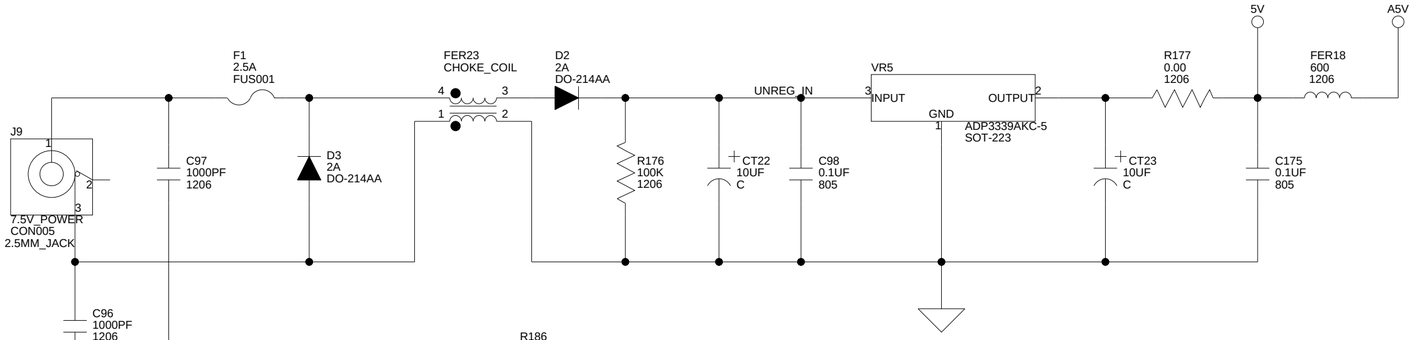
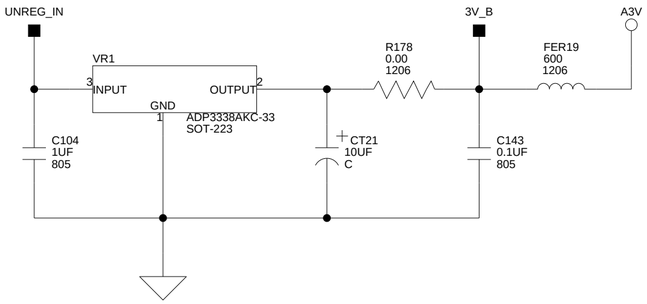
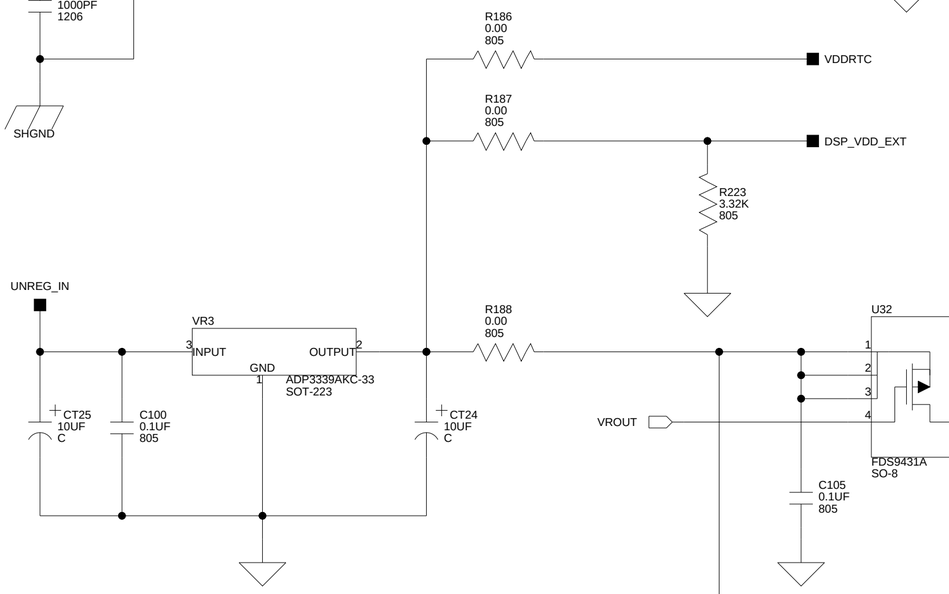
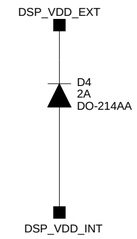




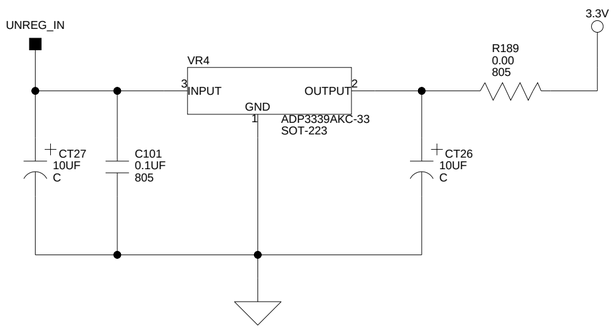


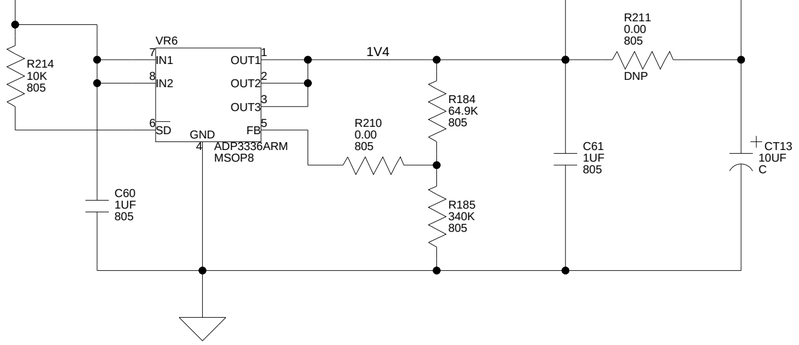


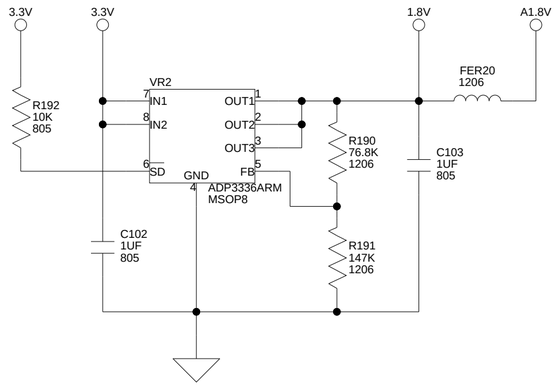
SW10: Core Voltage Source Select
DEFAULT: Not Populated

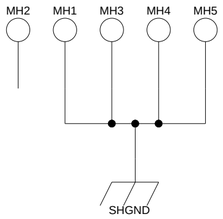
Position	Function
1 and 2	DSP_VDD_INT = DSP Internal Voltage Regulation
2 and 3	DSP_VDD_INT = 1.4V Fixed

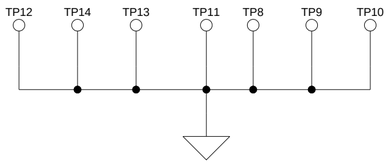
Note: For boards without a 750MHz processor this jumper will not be populated and the DSP_VDD_INT will be hard-wired with R222 to use the processor internal regulator.

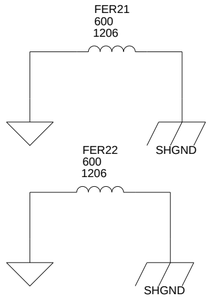












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Title: ADSP-BF533 EZ-KIT LITE - POWER

Size: C | Board No.: A0167-2001 | Rev: 1.6C

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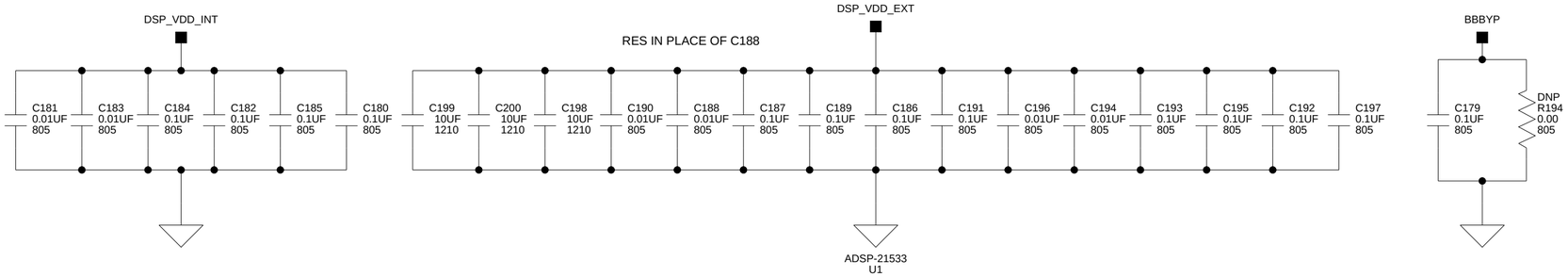

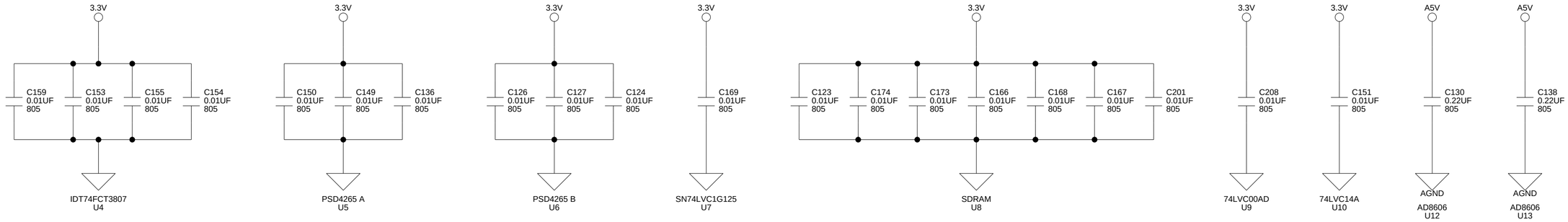

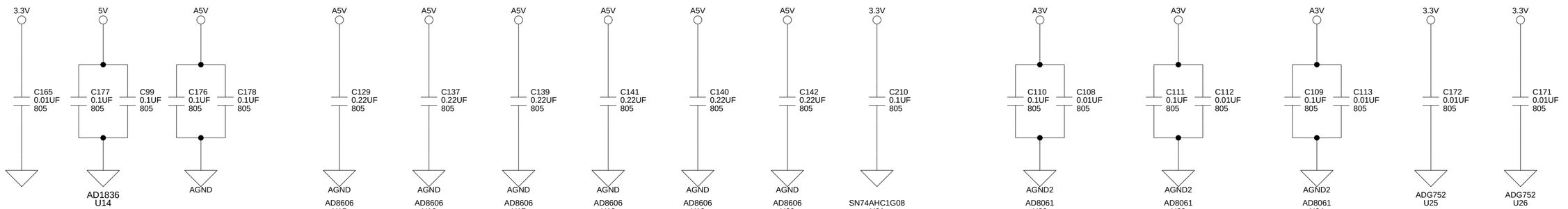

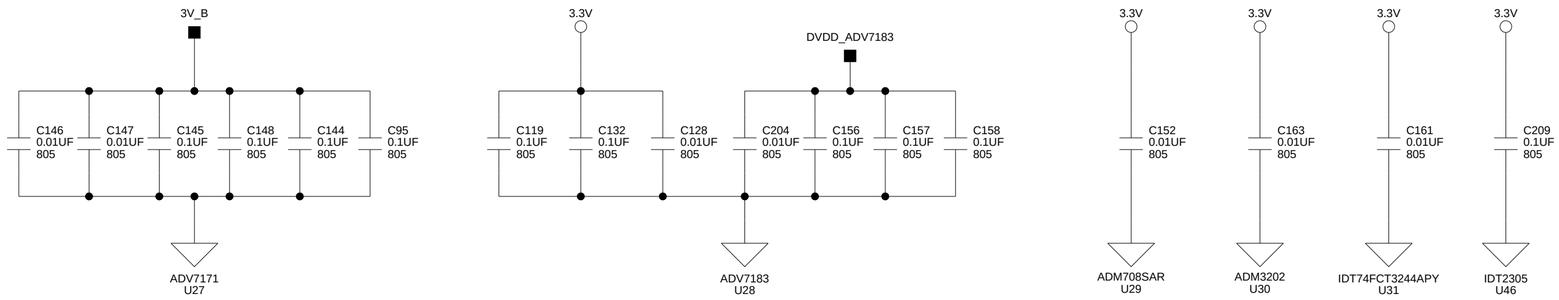

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Title: ADSP-BF533 EZ-KIT LITE - BYPASS CAPS

Size	Board No.	Rev
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