ARM®

The Architecture for the Digital World

- ARM is the world's leading semiconductor IP company *with 22 Million processors entering the market each day.*
  - 30 billion ARM processors shipped to date, 8 billion ARM-based chips in 2011 – 30% CAGR over last 5 years
  - Unrivalled Partner ecosystem
    - 850 processor licenses – growing by 100 annually
    - Millions of developers; billions of users
  - ARM has the right technology – optimized for a mobilizing world

ARM Founded 27th Nov 1990

- A barn, some energy, experience and belief: “We’re going to be the Global Standard”
- 13 engineers and a CEO, now >2,100
- Goal to design low power embedded 32bit processors, but to never build them
- 2½ decades of Partnership success

- 8 Partners in 1994

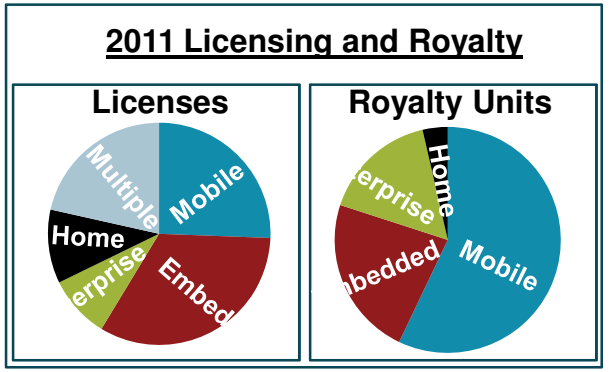
- 900+ Partners today

ARM Technology

- Advanced consumer products are incorporating more and more ARM technology – from processor and multimedia IP to software

Strong Growth in all Markets

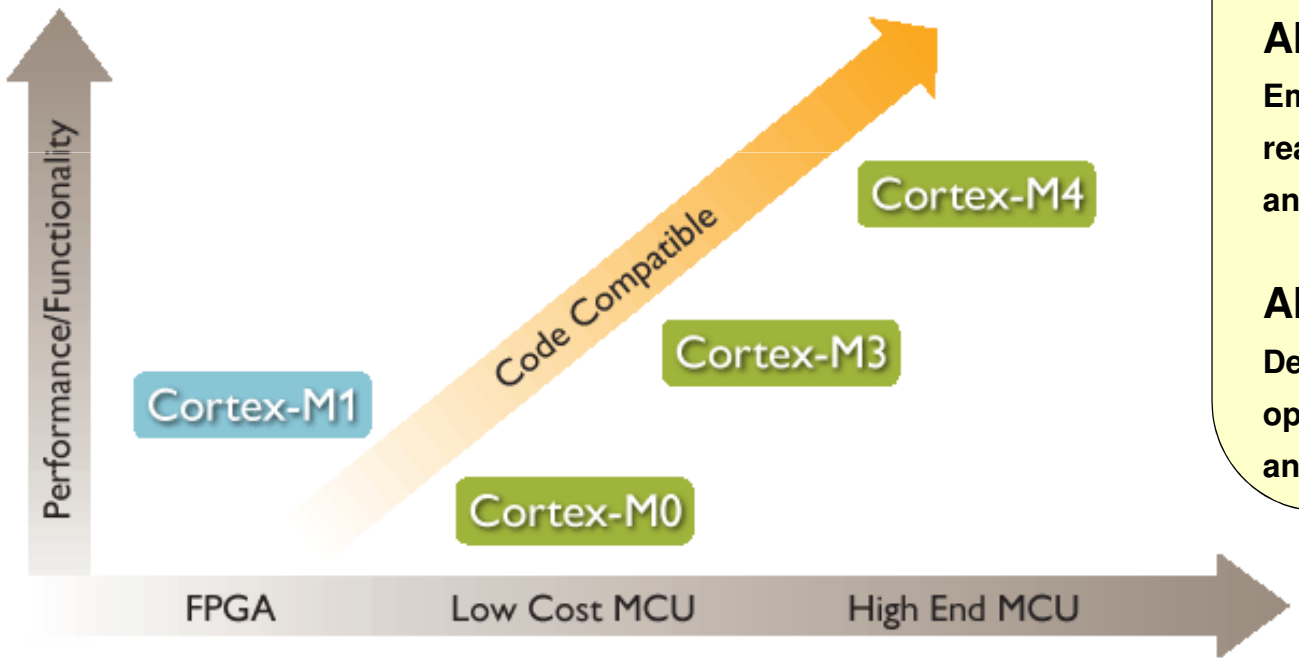
- Increasing penetration as semiconductor companies deploy ARM technology into broad range of end markets
- Mobile devices is still our largest market with embedded and enterprise the fastest growing



Cortex™-M Processor Portfolio

Cortex-M processor family

- **Seamless embedded architecture**
  - Spanning cost and performance points

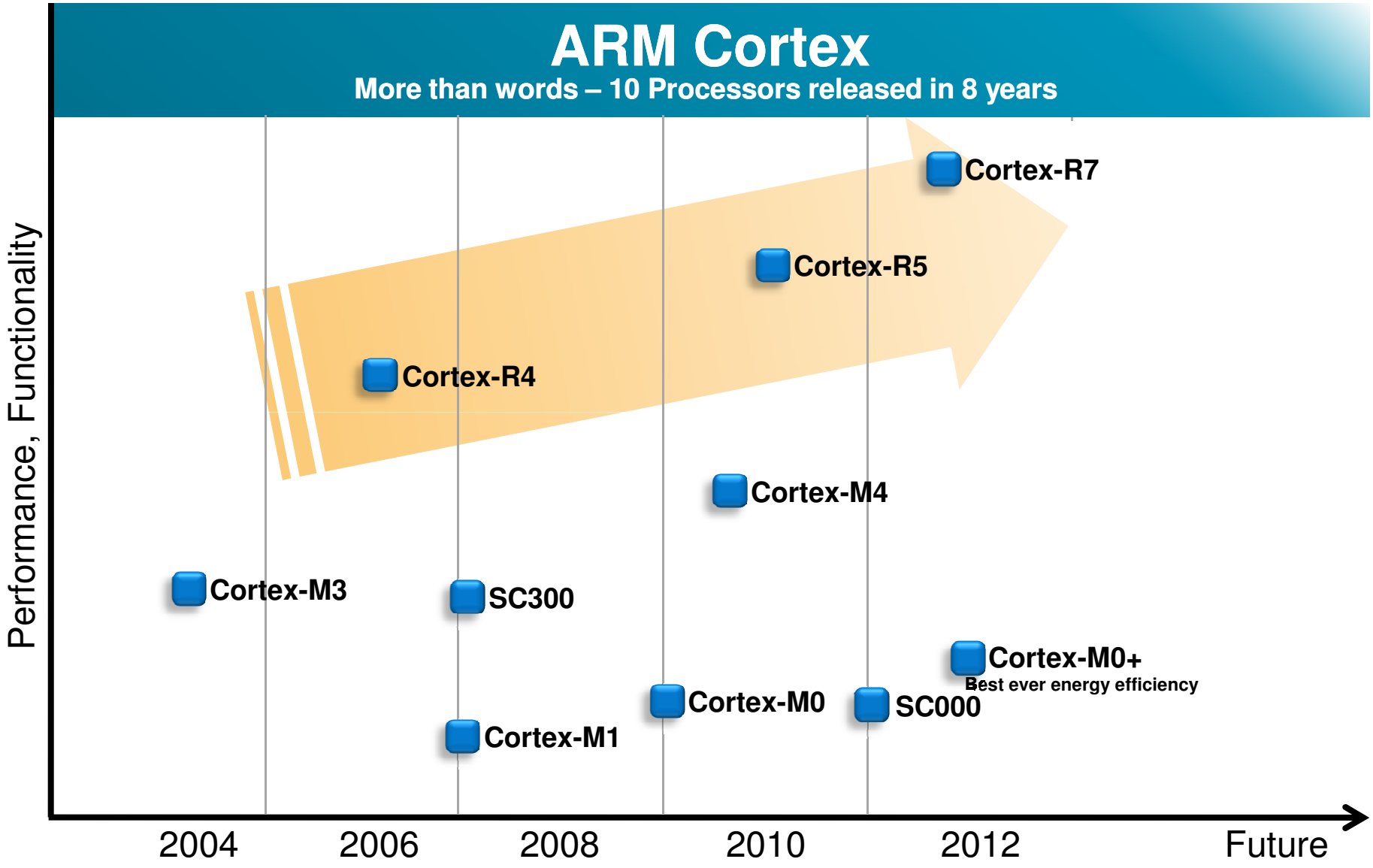


ARM Cortex-A Series:
Applications processors for feature-rich OS and user applications

ARM Cortex-R Series:
Embedded processors for real-time signal processing and control applications

ARM Cortex-M Series:
Deeply embedded processors optimized for microcontroller and low-power applications

ARM Commitment to Microcontrollers



Market challenges

- **More features at lower cost**
  - Increasing connectivity (e.g. USB, Ethernet, 802.15, NFC)
  - Drive for better code reuse
  - Analog devices with increasing processing and communication
- **Energy efficiency**
  - Wireless sensors, motor control, metering
- **8/16-bit running out of performance headroom**
  - As complexity rises so does frequency and memory requirement

Embedded market drivers/trends

- Connectivity
  - Connectivity becoming ubiquitous

Healthy software ecosystem required

- Smart technology
  - Observe/react to the environment

Real-time signal processing essential

- Energy efficiency
  - Green technology trends

More capability, but not higher MHz or mW!

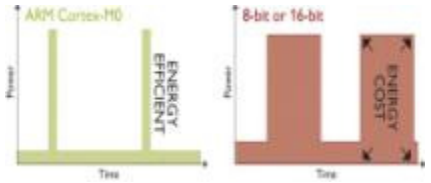
- Ease of use
  - Keep programming simple

Excellent tools required

Cortex-M processor solution

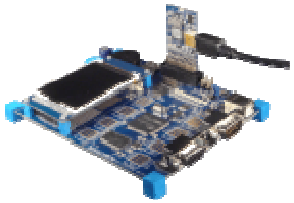
- **Energy efficiency**
  - Lower energy costs

Low power implementation
Sleep mode support
Wake-up Interrupt Controller
Increased intelligence at node



- **Ease of use**
  - Lower software costs

Broad tools and OS support
Binary compatible roadmap
Pure C target



- **High performance**
  - Competitive products

32-bit RISC architecture
High efficiency processor cores
Integrated Interrupt Controller (NVIC)

- **Reduced system cost**
  - Lower silicon costs

Thumb®-2 code density
Area optimised designs
CoreSight support

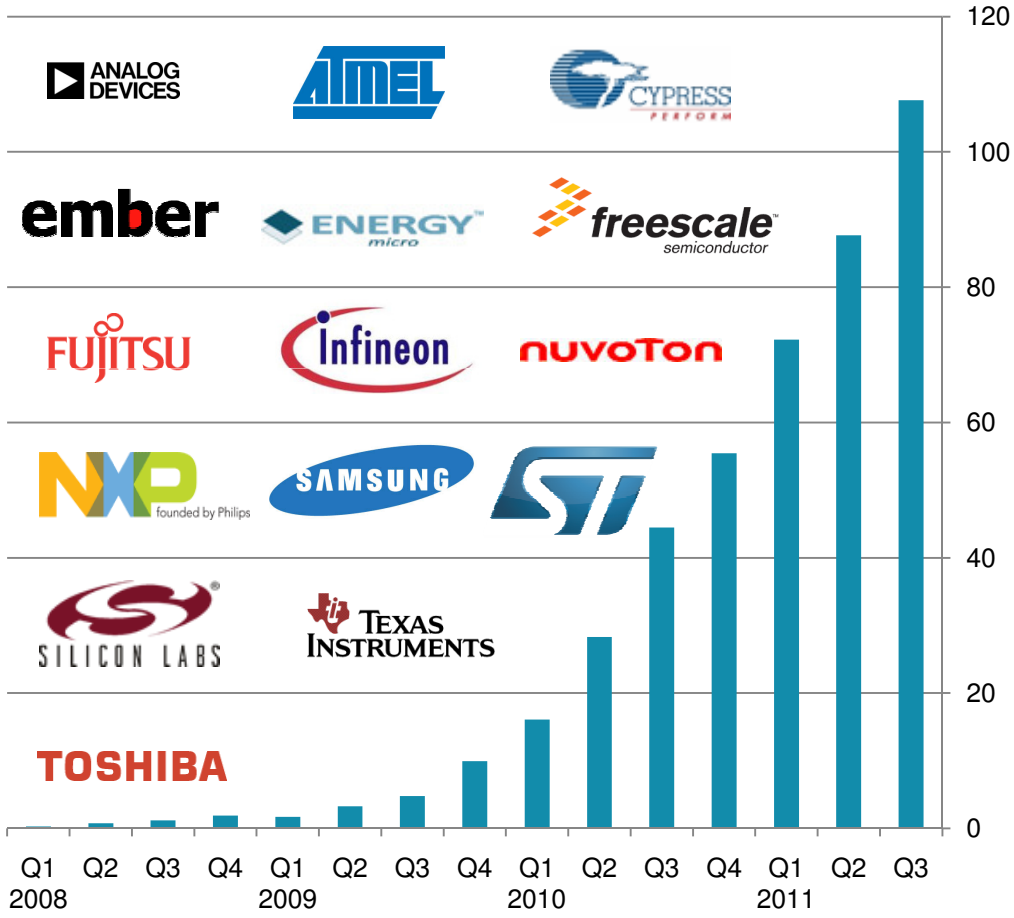
Cortex-M – Proven Success in Market

- 100+ licenses of ARM Cortex-M processors
- Over 1000 Cortex-M processor-based devices

Cortex-M Shipping >250Mu per Quarter

- **More than 10 partners in full production**
- **Additional licensees nearing ramp-up**
- **All Cortex-M Profiles are supporting the growth**
- **Serving all segments:**
  - Automotive
  - Consumer
  - Industrial
  - Metering
  - Telecom
  - White Goods

Total Cortex-M MCU Shipments
in Million Units per Quarter



Spanning the application range

- **Forget traditional 8/16/32-bit classifications**
  - Seamless architecture across all applications
  - Every product optimised for ultra low power systems

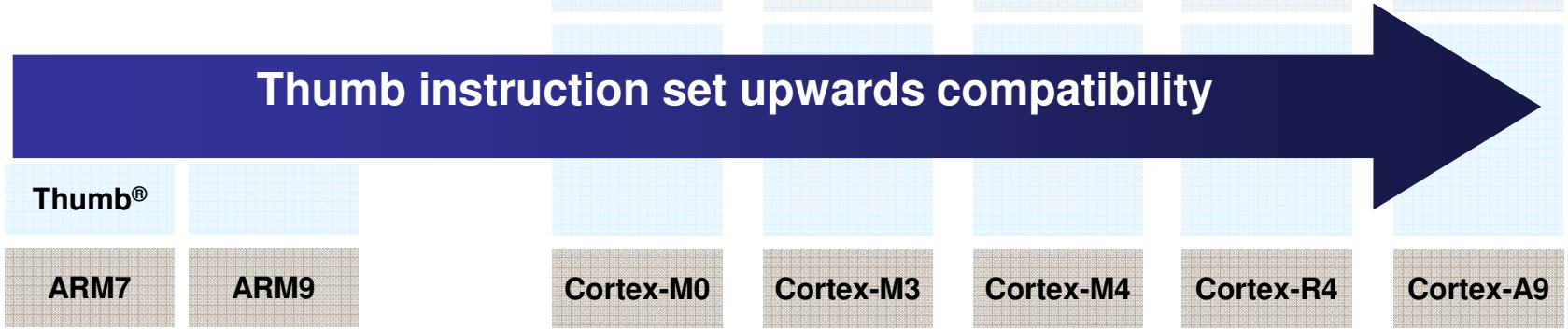
Cortex-M0	Cortex-M3	Cortex-M4
"8/16-bit" applications	"16/32-bit" applications	"32-bit/DSC" applications
Lowest cost Optimised connectivity	Performance efficiency Feature rich connectivity	MCU plus DSP Accelerated SIMD, FP & DSP



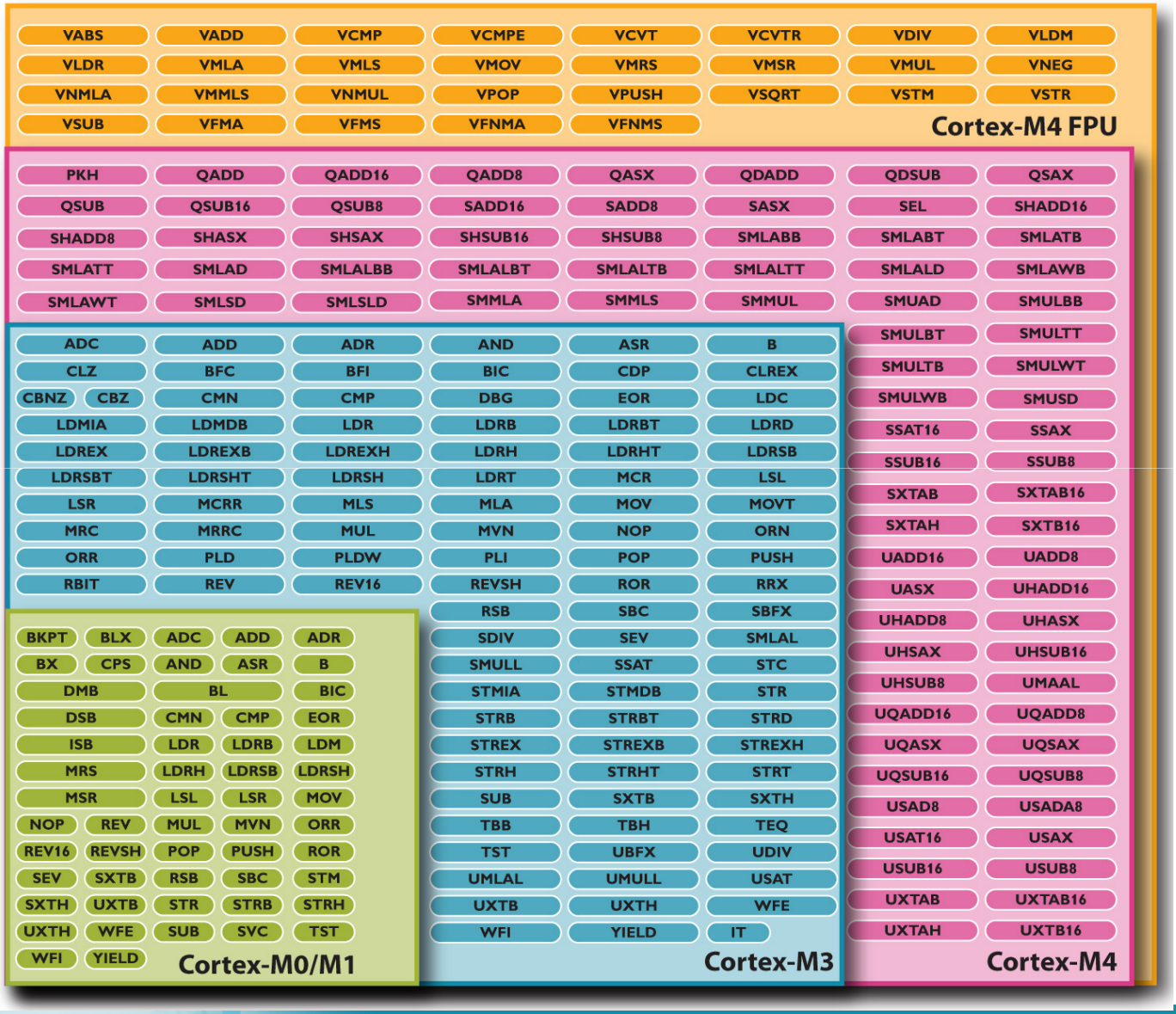



Instruction set architecture

- **Thumb**
  - 32-bit operations in 16-bit instructions
  - Introduced in ARM7TDMI® processor ('T' stands for Thumb)
  - Subsequently supported in every ARM processor developed since
- **Thumb-2**
  - Enables a performance optimised blend of 16/32-bit instructions
  - All processor operations can all be handled in 'Thumb' state
  - Supported across the Cortex-M processor range



Powerful Cortex-M instruction set



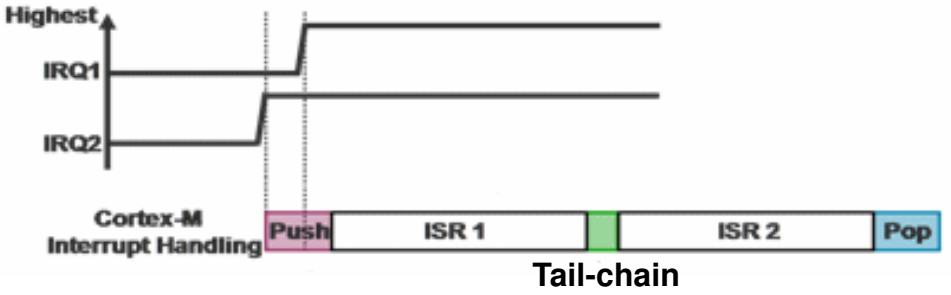
Nested Vectored Interrupt Controller

- **Faster interrupt response**
  - With less software effort

8051	Cortex-M
1. SJMP/L JMP from vector table to handler 2. PUSH PSW 3. ORL PSW, #00001000b (to switch register bank) 4. Starting real handler code	1. Starting real handler code

- **ISR written directly in C**
  - Interrupt table is simply a set of pointers to C routines
  - ISRs are standard C functions

- **Integrated NVIC handles:**
  - Saving corruptible registers
  - Exception prioritization
  - Exception nesting



Code density

- **Cortex-M shows smaller code size than 8/16-bit devices**
- **Consider a 16-bit multiply operation**
  - Required for 10-bit ADC data filtering, encryption algorithms, audio

8-bit example (8051)	16-bit example	ARM Cortex-M

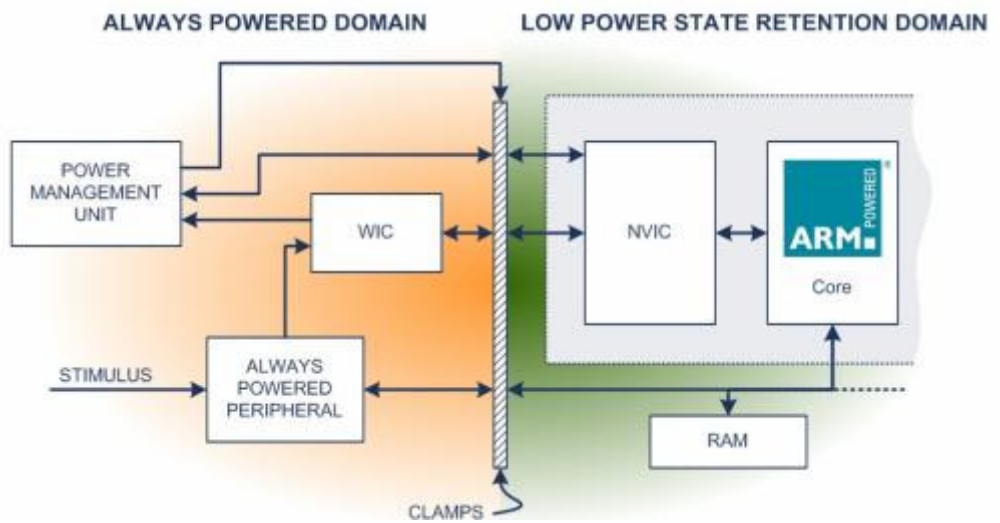
MOV A, XL ; 2 bytes
MOV B, YL ; 3 bytes
MUL AB; 1 byte
MOV R0, A; 1 byte
MOV R1, B; 3 bytes
MOV A, XL ; 2 bytes
MOV B, YH ; 3 bytes
MUL AB; 1 byte
ADD A, R1; 1 byte
MOV R1, A; 1 byte
MOV A, B ; 2 bytes
ADDC A, #0 ; 2 bytes
MOV R2, A; 1 byte
MOV A, XH ; 2 bytes
 	
MOV B, YL ; 3 bytes
 	
MUL AB; 1 byte
ADD A, R1; 1 byte
MOV R1, A; 1 byte
MOV A, B ; 2 bytes
ADDC A, R2 ; 1 bytes
MOV R2, A; 1 byte
MOV A, XH ; 2 bytes
MOV B, YH ; 3 bytes
MUL AB; 1 byte
ADD A, R2; 1 byte
MOV R2, A; 1 byte
MOV A, B ; 2 bytes
ADDC A, #0 ; 2 bytes
MOV R3, A; 1 byte
	MOV R1,&MulOp1
	MOV R2,&MulOp2
	MOV SumLo,R3
	MOV SumHi,R4
	
	(Memory mapped multiply unit)
		MULS r0,r1,r0

Time: 48 clock cycles* **Code size:** 48 bytes	**Time:** 8 clock cycles **Code size:** 8 bytes	**Time:** 1 clock cycle **Code size:** 2 bytes

* 8051 needs at least one cycle per instruction byte fetch as they only have an 8-bit interface

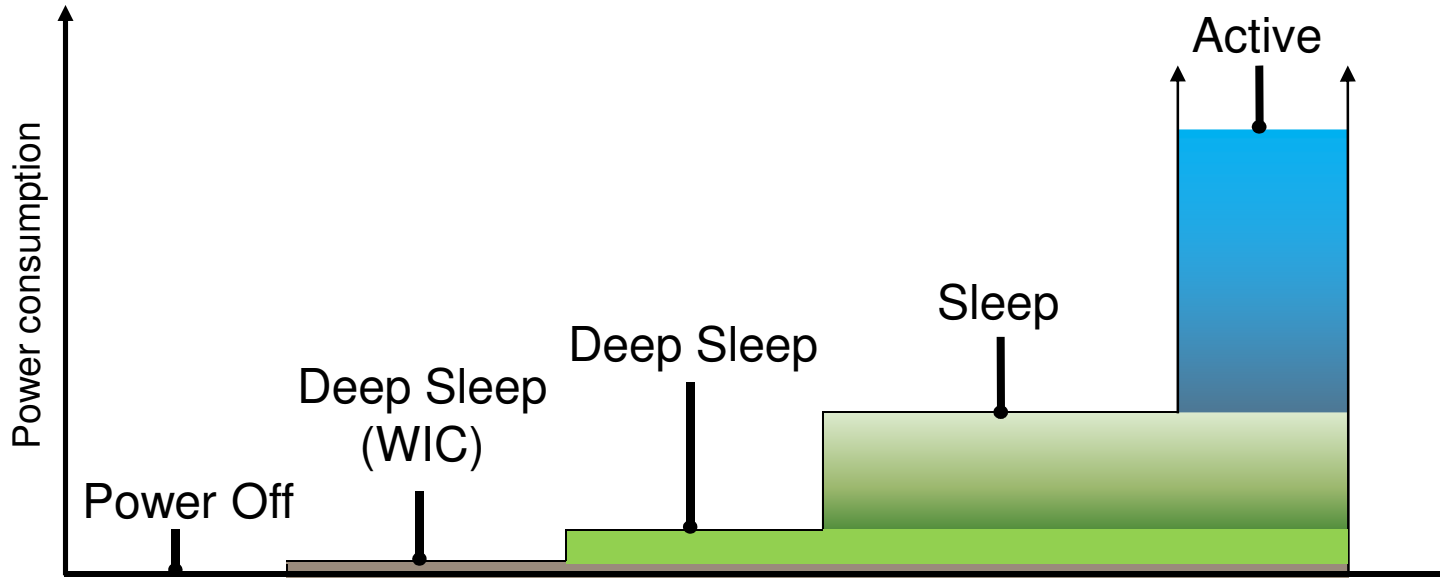
Cortex-M low power technologies

- All Cortex-M processors are specifically designed for low power, with a range of complementary technologies including:
- Integrated architectural clock gating
- Sleep and deep sleep modes:
  - puts the processor into a low-power state with flexible software control
- "Sleep-on-exit" interrupt handling:
  - enables the processor to sleep whenever all outstanding Interrupts are complete
- Wakeup Interrupt Controller (WIC)
  - enables advanced interrupt-controlled processing
  - enables nW power consumption in deep sleep mode with instant wakeup



Cortex-M Processor Power Modes

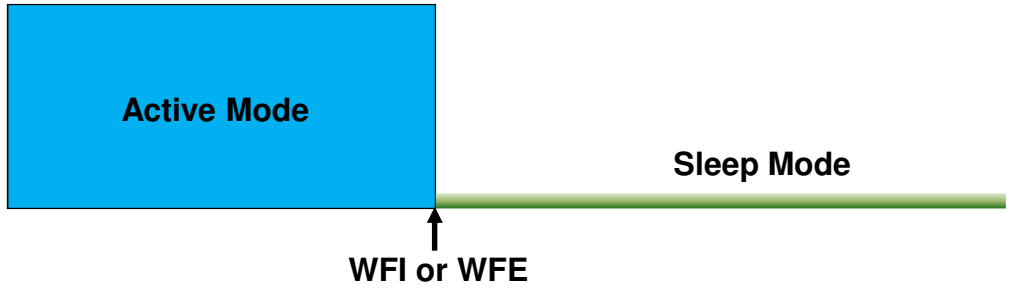
Active mode	Leakage + dynamic	Running Dhrystone 2.1 benchmark
Sleep mode	Leakage + some dynamic	Core clock gated, NVIC awake
Deep Sleep mode	Leakage only	Power still on, most clocks off
Deep Sleep mode	State retention (WIC)	Most power off, all clocks off
Power off	Zero power	Power off



Low Power Sleep Mode Features

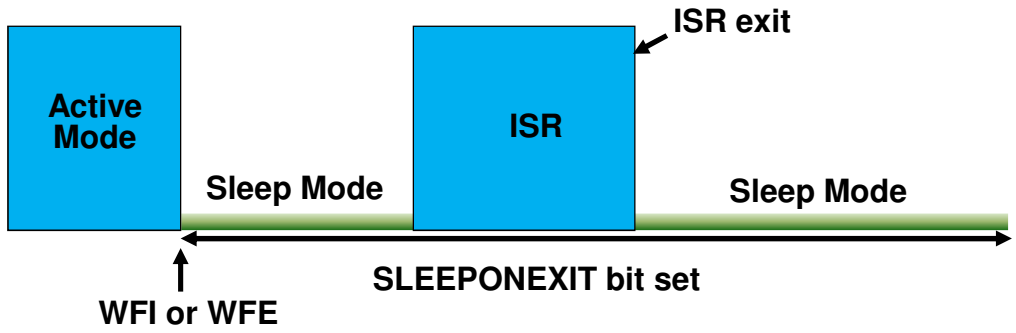
Sleep Now

Immediate sleep mode entry



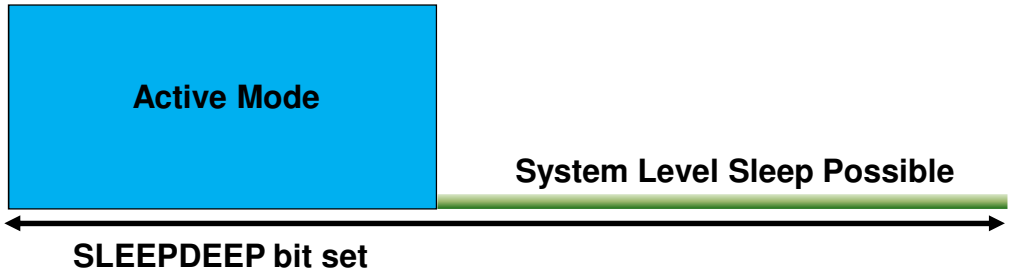
Sleep On Exit

Automatic sleep mode entry
on ISR service completion



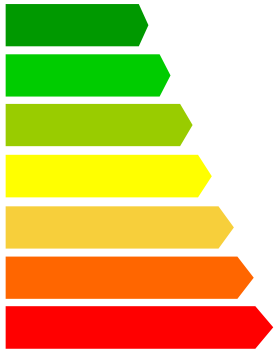
Deep Sleep

Communicate to system
that deeper sleep is possible



ARM Cortex-M0 Processor

- **Small, low power ARM processor**
  - A third of the area and power of ARM7TDMI-S™ processor
  - 12K gates, 47 µA/MHz in 180ULL with 0.9 DMIPS/MHz performance
  - Get to silicon faster with Cortex-M0 System Design Kit solution

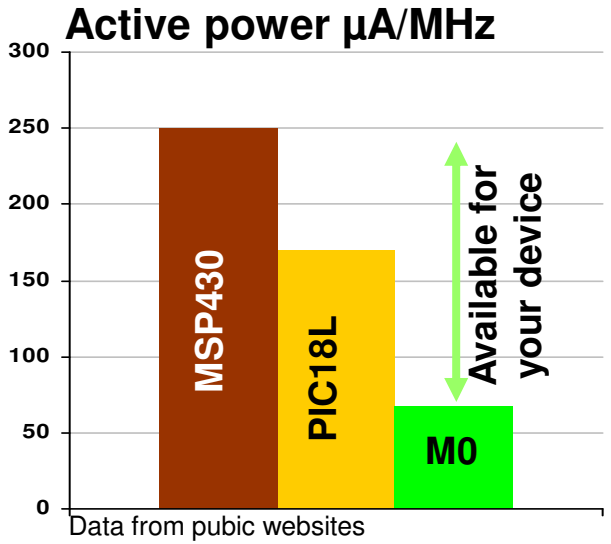


- Significant advantages over 8/16-bit
  - Longer battery life through energy efficiency
  - Reduced system cost through code density
  - Performance headroom for advanced features

- Extends ARM architecture to new applications
  - Ultra low-power MCU and mixed-signal devices
  - Ideal sequencer or FSM replacement on SoC
  - Upwards compatible with Cortex-M3 and Cortex-M4 processors

Efficiency with µA to spare

- **Cortex-M0 - extremely low power leakage and operation**
  - 67 µA/MHz active, 7nA state retention in full configuration*
  - Reduced Flash access and no speculative fetches
- **Dramatic energy efficiency advantage over 8/16-bit**
  - Over 2-4x shorter duty cycle than MSP430 and PIC18**
  - Working smarter, sleeping longer
- **Ideal in power optimised designs**

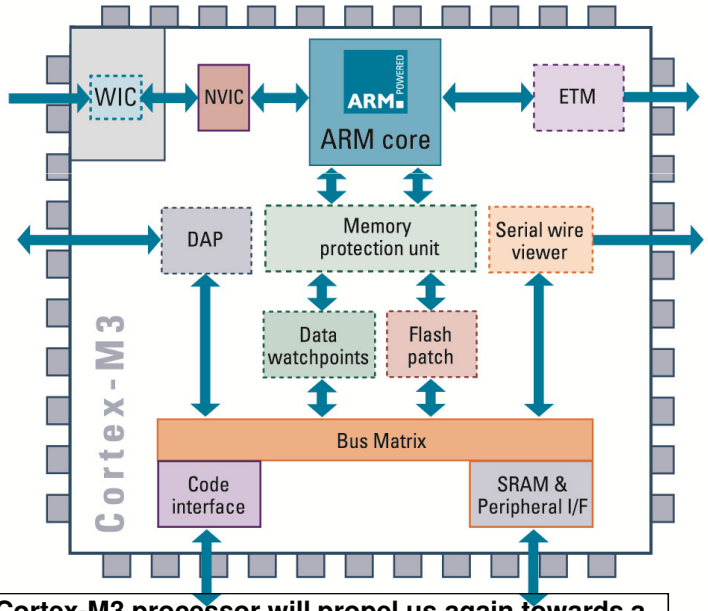


* Using ARM Physical IP with PMK on 180ULL process at 1.8V - ARM Cortex-M0 in full configuration (32 interrupts, fast mul, debug)

** Based on benchmarks in public domain.

Cortex-M3 processor - technical excellence

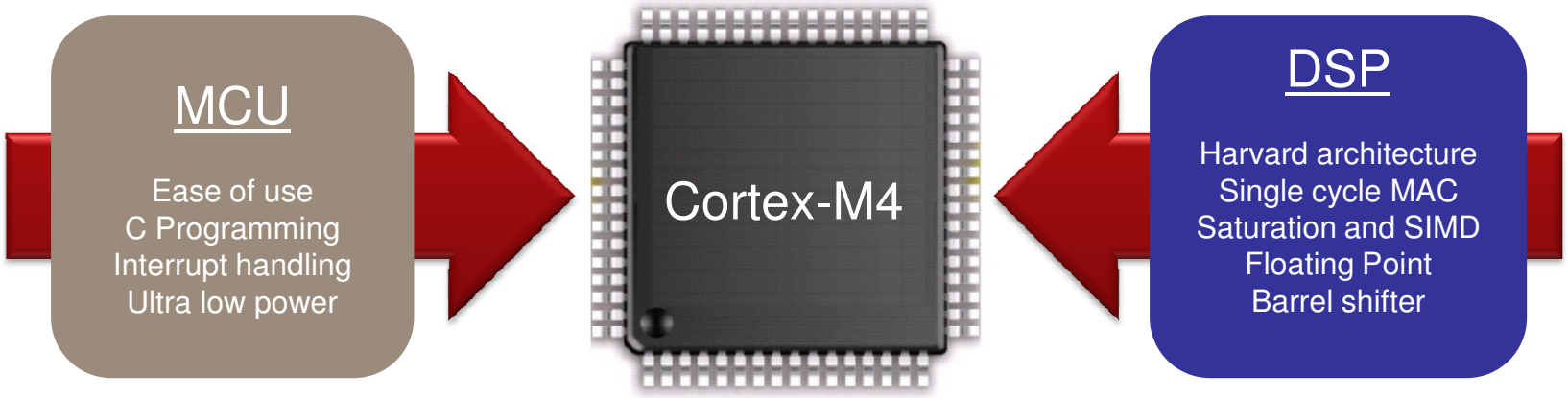
- Optimal performance, high efficiency processor core – 1.25 DMIPS/MHz
- Integrated bus matrix for increased performance
- Advanced power management features and capabilities
- Fully configurable to balance features and silicon area
  - Low latency, integrated Nested Vectored Interrupt Controller (NVIC)
  - Sophisticated debug and trace support
  - Memory Protection Unit (MPU)
  - Embedded Trace Macrocell (ETM)
  - Fault Robust Interface
- Launched 2004
  - Broad adoption within microcontroller and embedded SoC markets
- Rev2 released in 2008 with many new power management and configuration capabilities



"…. the Cortex-M3 processor will propel us again towards a breakthrough in performance, ease of use and quality, while also providing a competitive cost structure for our products. We feel that the Cortex M3 processor will play an important role in accelerating the convergence of the MCU market…"

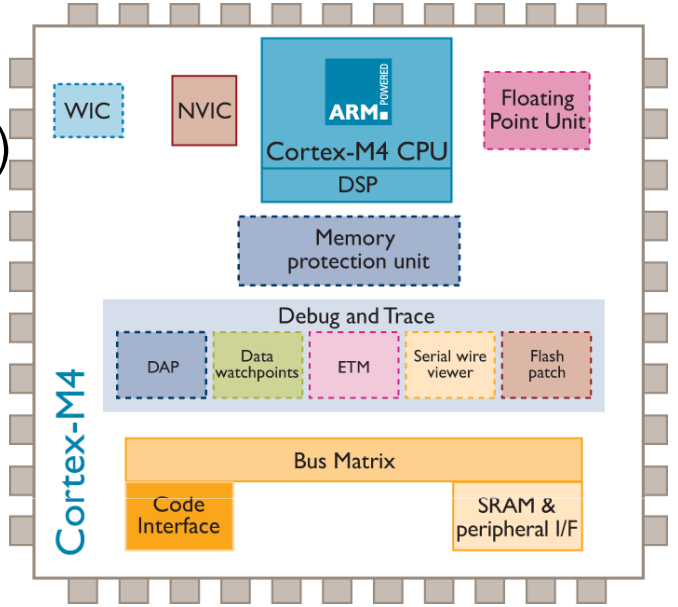
– Jim Nicholas, GM Microcontroller Division, ST

Cortex-M4 for digital signal control



Cortex-M4 processor details

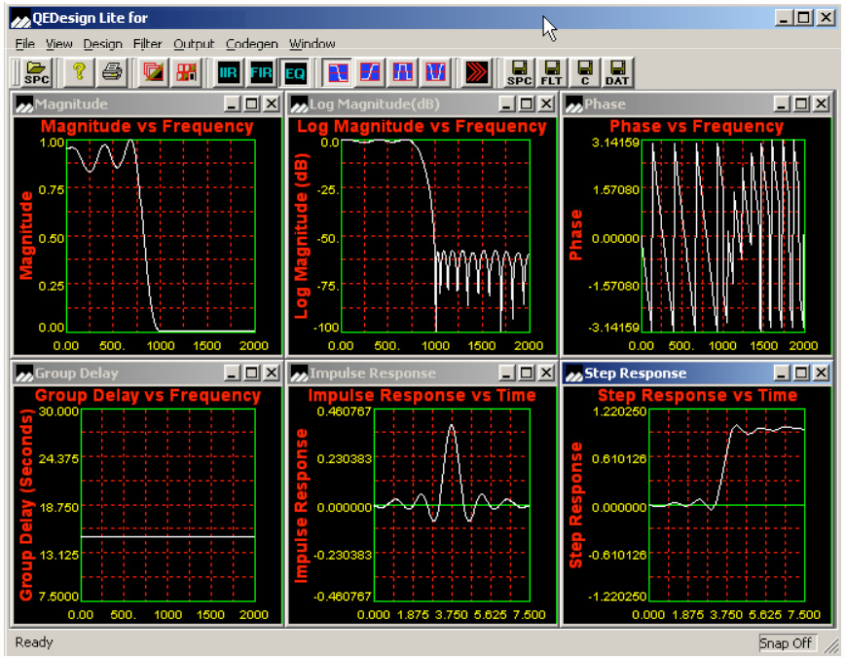
- **ARMv7ME architecture**
  - Thumb-2 technology
  - DSP extensions (with saturation and SIMD)
  - Single cycle MAC (Up to 32 x 32 + 64->64)
  - Optional decoupled single precision FPU
  - Integrated configurable NVIC
  - Compatible with Cortex-M3 processor
- **Microarchitecture**
  - 3-stage pipeline with branch speculation
  - 3x AMBA® AHB-Lite Bus Interfaces
- **Configurable for ultra low power**
  - Deep Sleep Mode, Wakeup Interrupt Controller
  - Power down features for the optional Floating Point Unit
- **Flexible configurations for wider applicability**
  - Configurable Interrupt Controller (1-240 Interrupts and Priorities)
  - Optional Memory Protection Unit, Optional Debug & Trace



Dotted boxes denote optional blocks

Cortex-M4 CMSIS extensions

- Cortex-M4 support available today in MDK-ARM and ARM Compiler
  - C Compiler intrinsic functions for Cortex-M4 extended Instructions
  - Optimized Floating Point Library using FPU CPU Instructions
  - Complete µVision Debugger support; including Instruction Set Simulation
- CMSIS - Expanded with Cortex-M4 Features (Intrinsic Functions)
  - Every CMSIS compliant C Compiler supports Cortex-M4 extensions
- Optimized CMSIS DSP Library
  - Designed to make DSP programs easy to develop for MCU users
  - **General Functions**
    math, trigonometric, control functions (building blocks)
  - **Digital Filter Algorithms**
    for filter design utilities and DSP toolkits (MathLab, LabVIEW, etc.)



Cortex-M feature set comparison

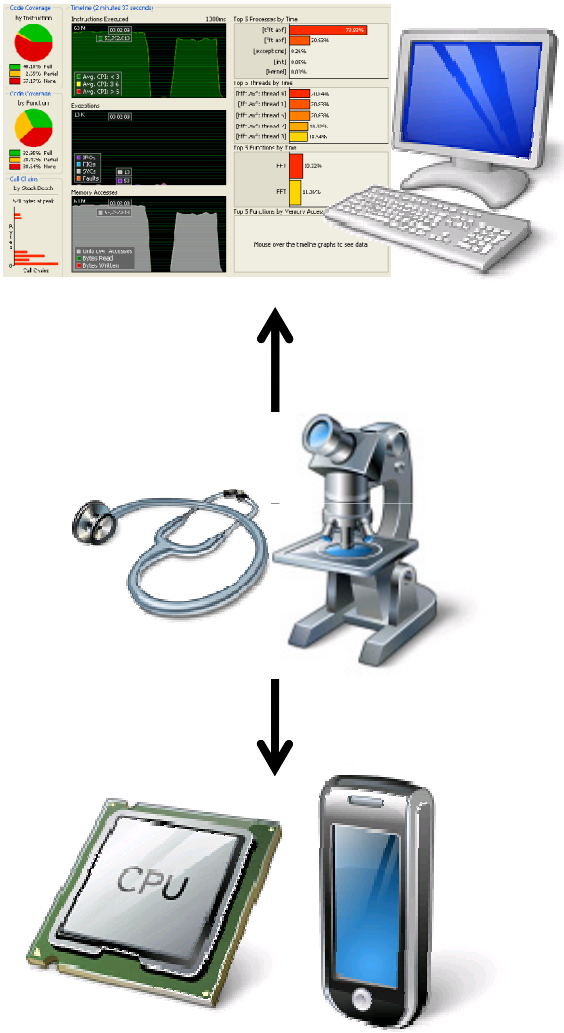
	ARM7TDMI	Cortex-M0	Cortex-M3	Cortex-M4
Instruction set architecture	ARM, Thumb	Thumb, Thumb-2 System Instructions	Thumb + Thumb-2	Thumb + Thumb-2, DSP, SIMD, FP
DMIPS/MHz	0.72 (Thumb), 0.95 (ARM)	0.9	1.25	1.25
CoreMark/MHz		1.62	2.17	2.19
Bus interfaces	1	1	3	3
Integrated NVIC	No	Yes	Yes	Yes
Number interrupts	2 (IRQ and FIQ)	1-32 + NMI	1-240 + NMI	1-240 + NMI
Interrupt priorities	None	4	8-256	8-256
Breakpoints, Watchpoints	2 Watchpoint Units	4/2/0, 2/1/0	8/4/0, 2/1/0	8/4/0, 2/1/0
Memory Protection Unit (MPU)	No	No	Yes (Option)	Yes (Option)
Integrated trace option (ETM)	Yes (Option)	No	Yes (Option)	Yes (Option)
Single Cycle Multiply	No	Yes (Option)	Yes	Yes
Hardware Divide	No	No	Yes	Yes
WIC Support	No	Yes	Yes	Yes
Bit banding support	No	System option	Yes (Option)	Yes (Option)
Single cycle DSP/SIMD	No	No	No	Yes
Floating point hardware	No	No	No	Yes
Bus protocol	Use AHB bus wrapper	AHB Lite	AHB Lite, APB	AHB Lite, APB
CMSIS Support	No	Yes	Yes	Yes

CoreSight
Debug and Trace Technology

CoreSight™
Debug & Trace IP by ARM

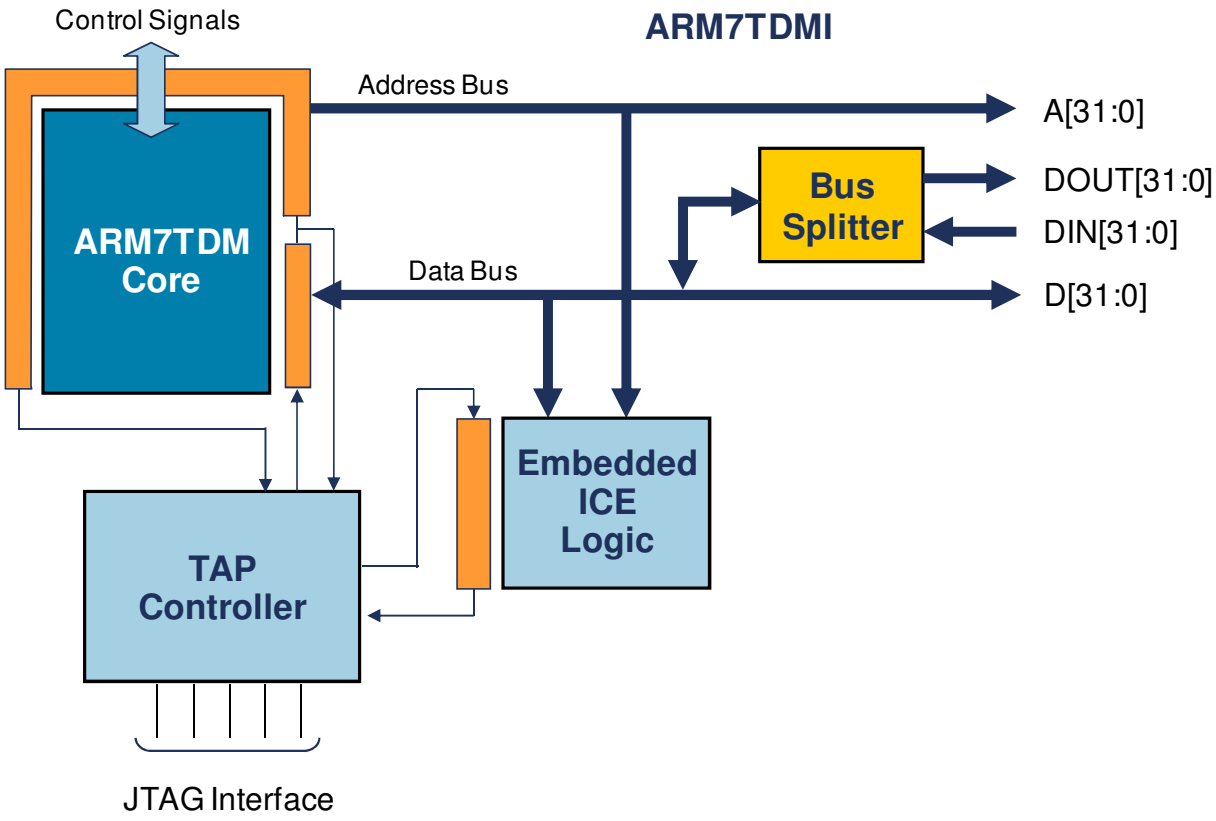
What is CoreSight?

- ARM's debug & trace architecture
  - Provides visibility and control of entire system
  - Used for hardware and software design & optimization
  - Modular, flexible architecture supporting ARM and other IP
  - Industry standard with established standards and comprehensive tool support
- CoreSight history
  - Embedded ICE logic conceived as a replacement for in circuit emulators in early 1990s
  - Real-time trace (ETM logic) introduced in late 1990s
- CoreSight looking forward
  - Providing system visibility to all for the devices of the future



CoreSight in the beginning...

- Debug on an ARM7
  - Embedded ICE logic with JTAG access



CoreSight in today's systems

- Example of debug and trace on a consumer device
  - CoreSight debug logic and trace logic in orange & green

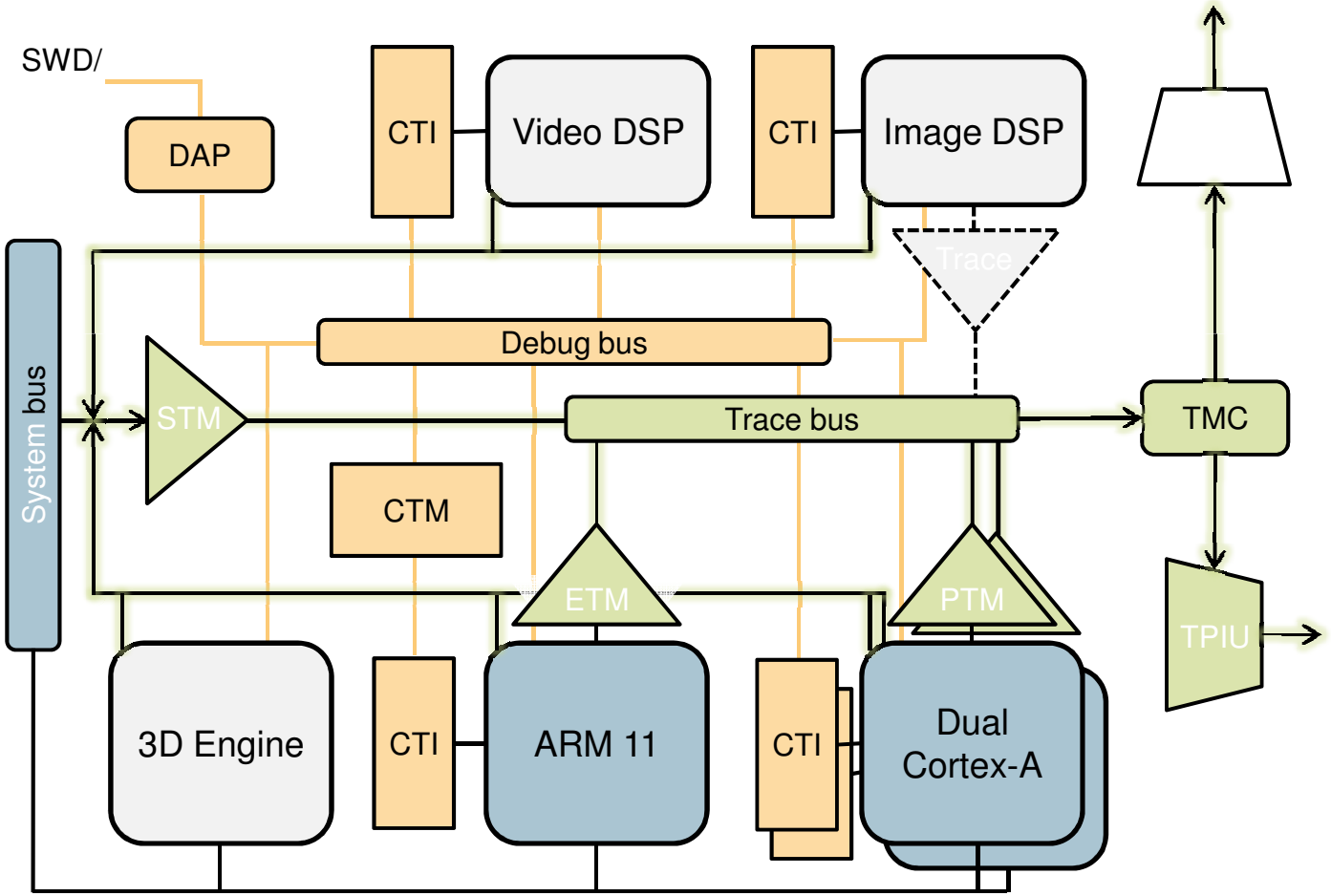
Dedicated debug & trace buses

CoreSight logic controlled via *Debug Access Port*

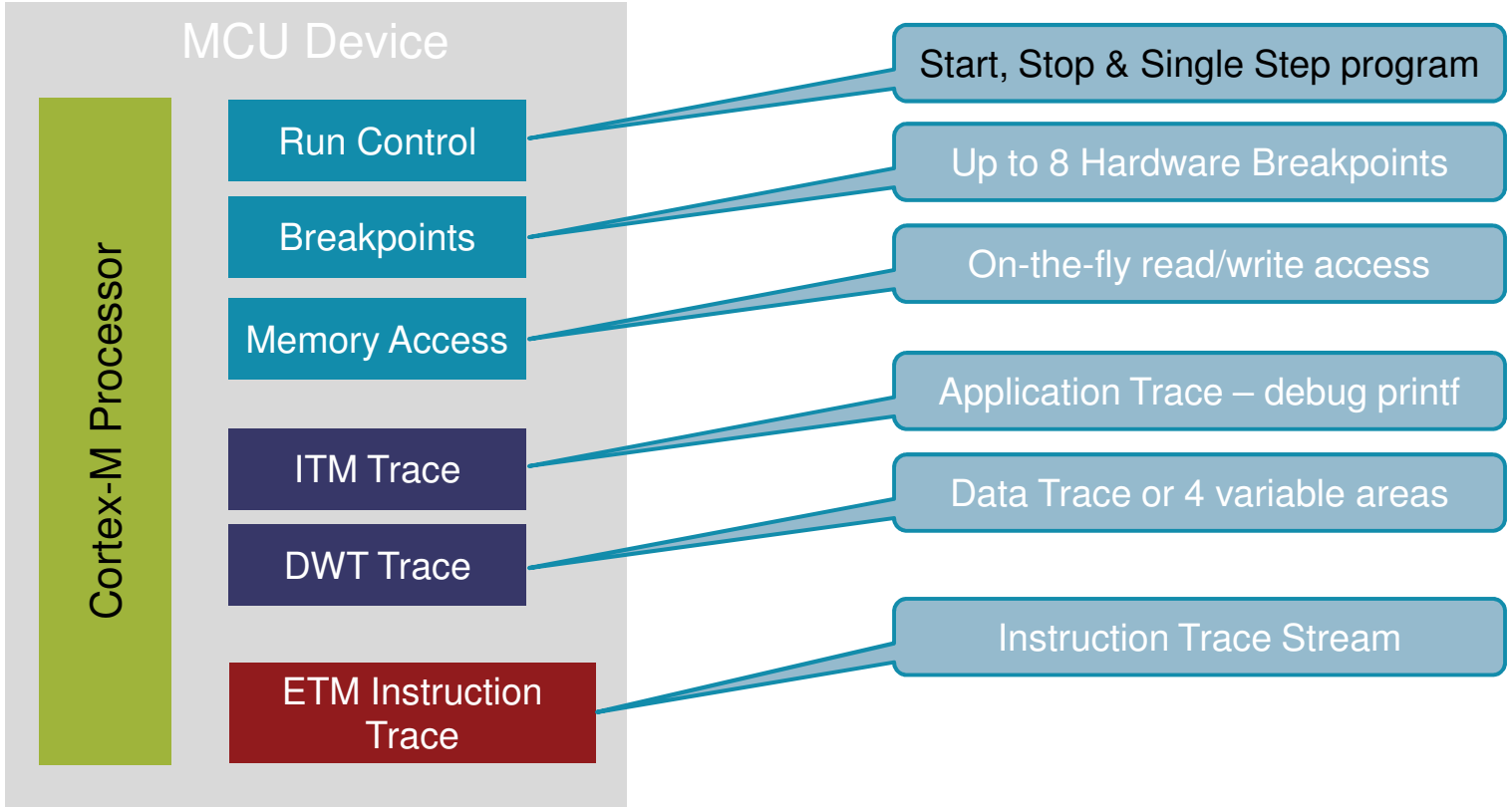
Cross-Trigger Matrix allows system-wide start/stop debug

ETM & *PTM* for processor trace. *STM* for system-wide trace

Trace Memory Controller can be used to re-route trace output

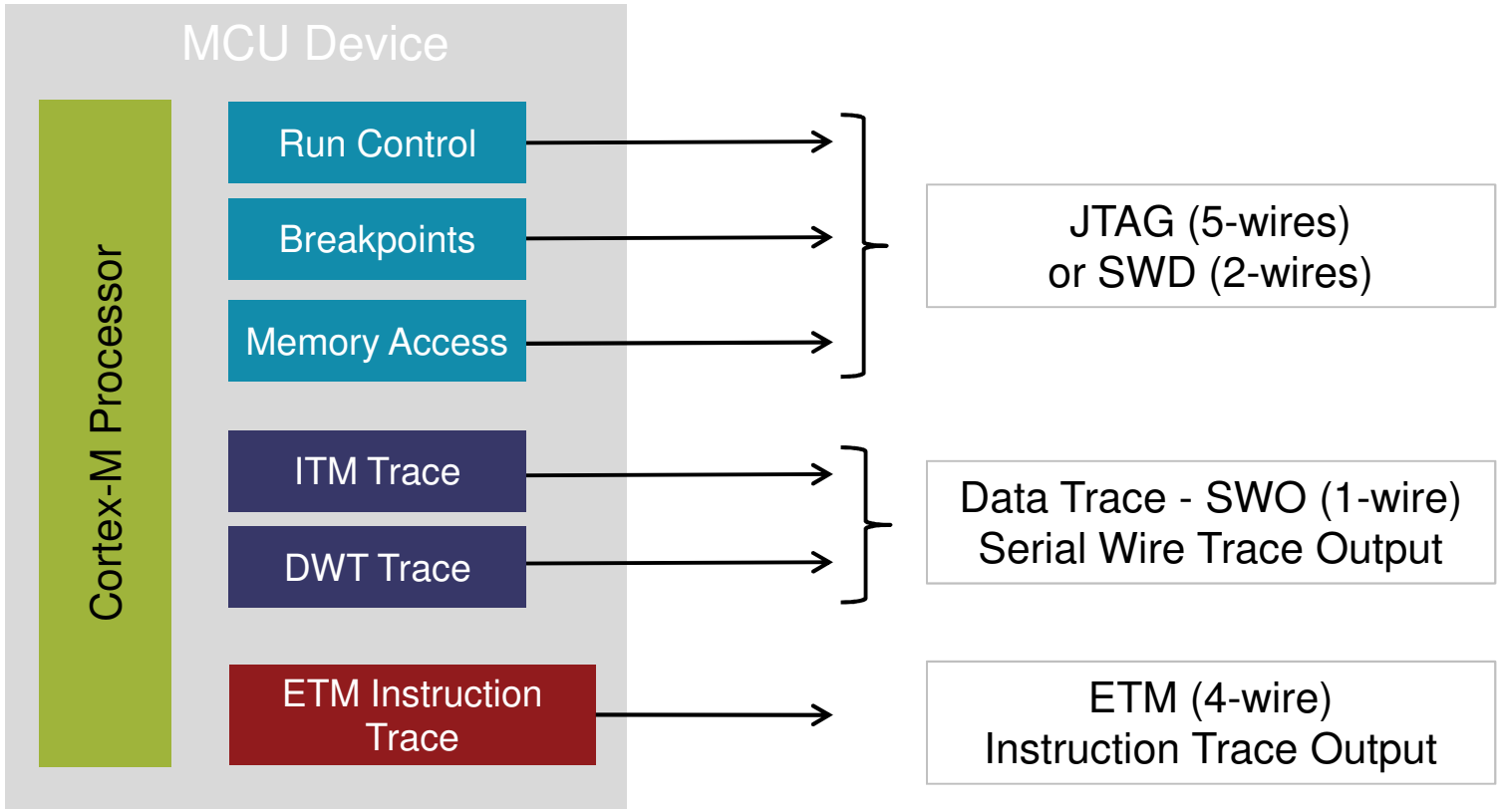


Cortex-M CoreSight



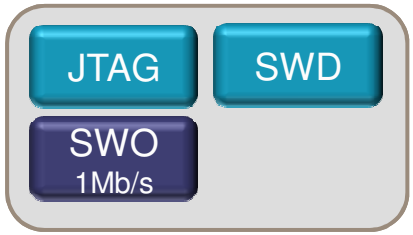
- CoreSight delivers comprehensive debug and trace in all Cortex-M MCUs
- ULINK handles this information
- µVision displays information for debug and analysis

Cortex-M CoreSight Interfaces



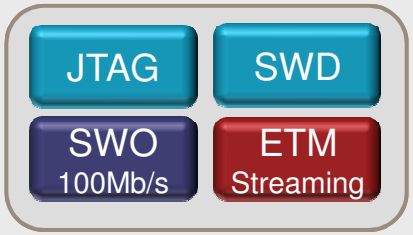
- SWD – Serial Wire Debug
- SWO – Serial Wire Output (data trace)
- ETM – Embedded Trace Macrocell

Debug and Trace Adapters



ULINK2:

- Programming + Run-Control
- Memory + Breakpoint Access
- Serial Wire Trace Capturing (SWO)
  - 1Mbit/sec (UART mode)



ULINK*pro*:

- Serial Wire Trace (SWO)
  - 100Mbit/sec (Manchester Mode)
- ETM Streaming Trace
  - Up to 800Mbit/sec
  - 100% Code Coverage and Performance Analysis

MDK-ARM : MCU Tools from ARM

- Tailored to ARM® Cortex-M™ devices
  - Optimized Compiler, IDE, Debugger, and Debug/Trace Adapters
  - Support for advanced Cortex-M and CoreSight™ technologies
  - RTOS and middleware optimized for Cortex-M devices

- Start projects faster
  - Device Database provides tool setup, start-up code, header files, flash algorithm, etc.
- Find and resolve code issues quickly
  - Make use of debug features such as Logic analyzer, RTOS aware views and conditional breakpoints
- Efficiently verify and optimize software
  - ULINK*pro* with Streaming Trace provides Code Coverage and Performance Analyzer