



## MC13192/MC13193



(Scale 1:1)

### Package Information

Plastic Package

Case 1311-03

(QFN-32)

### Ordering Information

| Device  | Device Marking | Package |
|---------|----------------|---------|
| MC13192 | 13192          | QFN-32  |
| MC13193 | 13193          | QFN-32  |

# MC13192/MC13193

## 2.4 GHz Low Power Transceiver for the IEEE<sup>®</sup> 802.15.4 Standard

### 1 Introduction

The MC13192 and MC13193 are short range, low power, 2.4 GHz Industrial, Scientific, and Medical (ISM) band transceivers. The MC13192/MC13193 contain a complete 802.15.4 physical layer (PHY) modem designed for the IEEE<sup>®</sup> 802.15.4 wireless standard which supports peer-to-peer, star, and mesh networking.

The MC13192 includes the 802.15.4 PHY/MAC for use with the HCS08 Family of MCUs. The MC13193 also includes the 802.15.4 PHY/MAC plus the ZigBee Protocol Stack for use with the HCS08 Family of MCUs. With the exception of the addition of the ZigBee Protocol Stack, the MC13193 functionality is the same as the MC13192.

When combined with an appropriate microcontroller (MCU), the MC13192/MC13193 provide a cost-effective solution for short-range data links and networks. Interface with the MCU is accomplished using a four wire serial peripheral interface (SPI) connection and an interrupt request output which allows for the use of a variety of processors. The software and processor

### Contents

|                              |    |
|------------------------------|----|
| 1 Introduction               | 1  |
| 2 Features                   | 2  |
| 3 Block Diagrams             | 3  |
| 4 Data Transfer Modes        | 3  |
| 5 Electrical Characteristics | 8  |
| 6 Functional Description     | 12 |
| 7 Pin Connections            | 15 |
| 8 Applications Information   | 18 |
| 9 Packaging Information      | 23 |

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

© Freescale Semiconductor, Inc., 2004, 2005. All rights reserved.

can be scaled to fit applications ranging from simple point-to-point systems, through complete ZigBee™ networking.

For more detailed information about MC13192/MC13193 operation, refer to the *MC13192/MC13193 Reference Manual*, part number MC13192RM.

Applications include, but are not limited to, the following:

- Remote control and wire replacement in industrial systems such as wireless sensor networks
- Factory automation and motor control
- Energy Management (lighting, HVAC, etc.)
- Asset tracking and monitoring

Potential consumer applications include:

- Home automation and control (lighting, thermostats, etc.)
- Human interface devices (keyboard, mice, etc.)
- Remote entertainment control
- Wireless toys

The transceiver includes a low noise amplifier, 1.0 mW power amplifier (PA), voltage controlled oscillator (VCO), on-board power supply regulation, and full spread-spectrum encoding and decoding. The device supports 250 kbps Offset-Quadrature Phase Shift Keying (O-QPSK) data in 2.0 MHz channels with 5.0 MHz channel spacing per the IEEE 802.15.4 specification. The SPI port and interrupt request output are used for receive (RX) and transmit (TX) data transfer and control.

## 2 Features

- Recommended power supply range: 2.0 to 3.4 V
- 16 Channels
- 0 dBm nominal, programmable from -27 dBm to 4 dBm typical maximum output power
- Buffered transmit and receive data packets for simplified use with low cost MCUs
- Supports 250 kbps O-QPSK data in 5.0 MHz channels and full spread-spectrum encode and decode (compatible with IEEE Standard 802.15.4)
- Three power down modes for power conservation:
  - < 1  $\mu$ A Off current
  - 1  $\mu$ A Typical Hibernate current
  - 35  $\mu$ A Typical Doze current (no CLKO)
- RX sensitivity of -92 dBm (typical) at 1.0% packet error rate
- Four internal timer comparators available to reduce MCU resource requirements
- Programmable frequency clock output for use by MCU
- Onboard trim capability for 16 MHz crystal reference oscillator eliminates need for external variable capacitors and allows for automated production frequency calibration.
- Seven general purpose input/output (GPIO) signals

- Operating temperature range: -40 °C to 85 °C
- Small form factor QFN-32 Package
  - RoHS compliant
  - Meets moisture sensitivity level (MSL) 3
  - 260 °C peak reflow temperature
  - Meets lead-free requirements

## 3 Block Diagrams

Figure 3 shows a simplified block diagram of the MC13192/MC13193 which is an IEEE Standard 802.15.4 compatible transceiver that provides the functions required in the physical layer (PHY) specification. Figure 4 shows the basic system block diagram for the MC13192/MC13193 in an application. Interface with the transceiver is accomplished through a 4-wire SPI port and interrupt request line. The media access control (MAC), drivers, and network and application software (as required) reside on the host processor. The host can vary from a simple 8-bit device up to a sophisticated 32-bit processor depending on application requirements.

## 4 Data Transfer Modes

The MC13192/MC13193 has two data transfer modes:

1. Packet Mode — Data is buffered in on-chip RAM
2. Streaming Mode — Data is processed word-by-word

The Freescale 802.15.4 MAC software only supports the streaming mode of data transfer. For proprietary applications, packet mode can be used to conserve MCU resources.

### 4.1 Packet Structure

Figure 5 shows the packet structure of the MC13192/MC13193. Payloads of up to 125 bytes are supported. The MC13192/MC13193 adds a four-byte preamble, a one-byte Start of Frame Delimiter (SFD), and a one-byte Frame Length Indicator (FLI) before the data. A two-byte Frame Check Sequence (FCS) is calculated and appended to the end of the data.

## 4.2 Receive Path Description

In the receive signal path, the RF input is converted to low IF In-phase and Quadrature (I & Q) signals through two down-conversion stages. A Clear Channel Assessment (CCA) can be performed based upon the baseband energy integrated over a specific time interval. The digital back end performs Differential Chip Detection (DCD), the correlator “de-spreads” the Direct Sequence Spread Spectrum (DSSS) Offset QPSK (O-QPSK) signal, determines the symbols and packets, and detects the data.

The preamble, SFD, and FLI are parsed and used to detect the payload data and FCS which are stored in RAM. A two-byte FCS is calculated on the received data and compared to the FCS value appended to the transmitted data, which generates a Cyclical Redundancy Check (CRC) result. Link Quality is measured over a 64  $\mu$ s period after the packet preamble and stored in RAM.

If the MC13192/MC13193 is in packet mode, the data is processed as an entire packet. The MCU is notified that an entire packet has been received via an interrupt.

If the MC13192/MC13193 is in streaming mode, the MCU is notified by an interrupt on a word-by-word basis.

Figure 1 shows CCA reported power level versus input power. Note that CCA reported power saturates at about -57 dBm input power which is well above IEEE 802.15.4 Standard requirements. Figure 2 shows energy detection/LQI reported level versus input power. Note that for both graphs the required IEEE 802.15.4 Standard accuracy and range limits are shown.

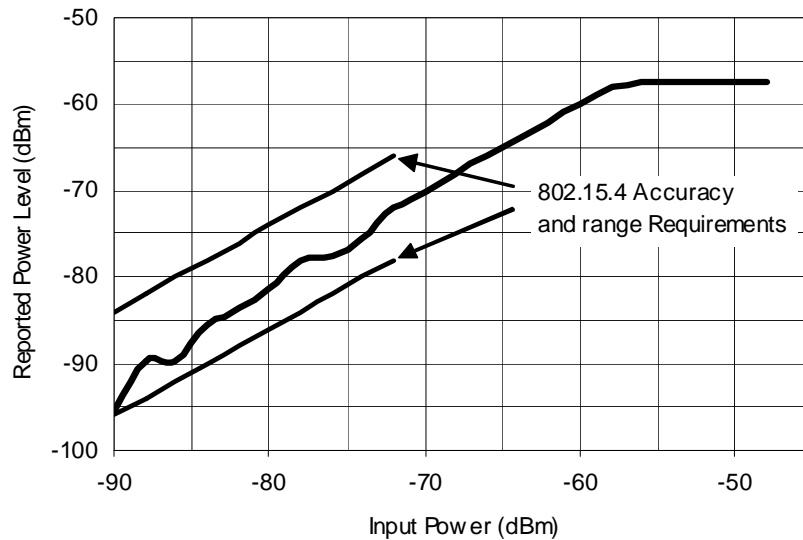
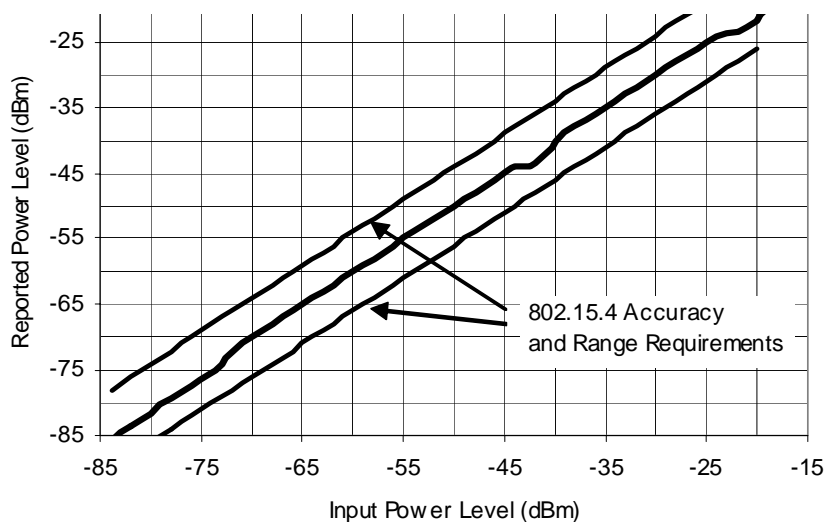


Figure 1. Reported Power Level versus Input Power in Clear Channel Assessment Mode



**Figure 2. Reported Power Level Versus Input Power for Energy Detect or Link Quality Indicator**

### 4.3 Transmit Path Description

For the transmit path, the TX data that was previously stored in RAM is retrieved (packet mode) or the TX data is clocked in via the SPI (stream mode), formed into packets per the 802.15.4 PHY, spread, and then up-converted to the transmit frequency.

If the MC13192/MC13193 is in packet mode, data is processed as an entire packet. The data is first loaded into the TX buffer. The MCU then requests that the MC13192/MC13193 transmit the data. The MCU is notified via an interrupt when the whole packet has successfully been transmitted.

In streaming mode, the data is fed to the MC13192/MC13193 on a word-by-word basis with an interrupt serving as a notification that the MC13192/MC13193 is ready for more data. This continues until the whole packet is transmitted.

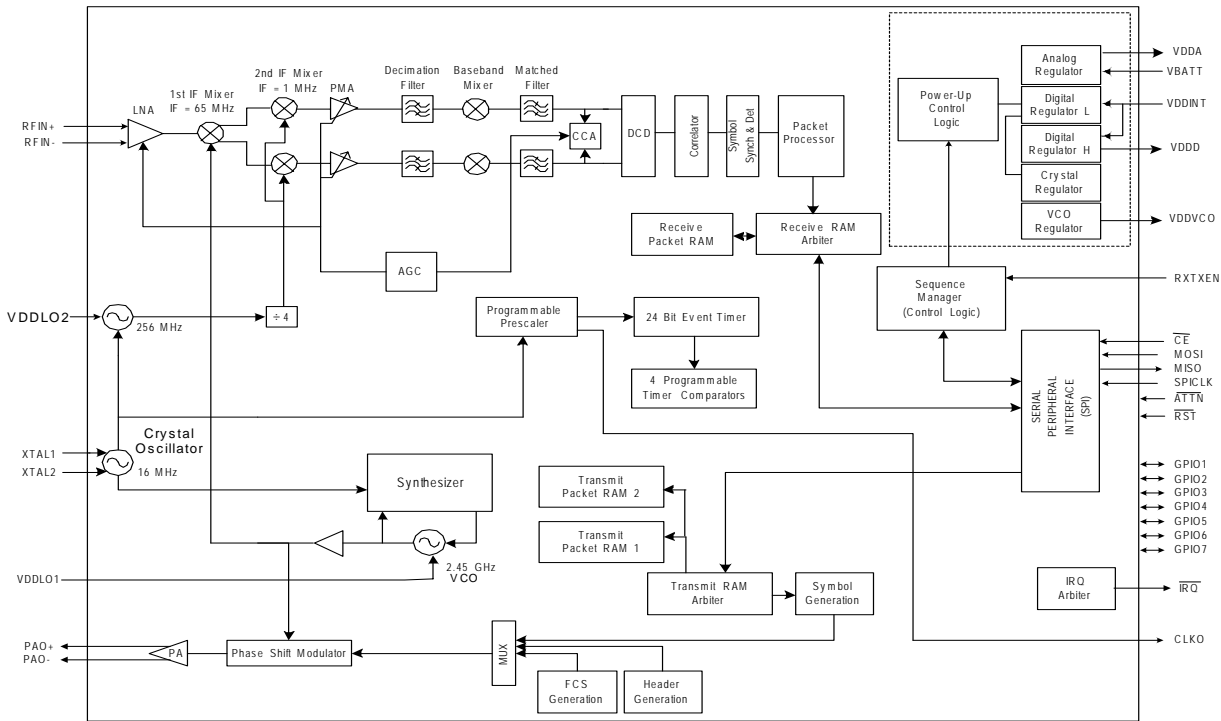


Figure 3. MC13192 Simplified Block Diagram

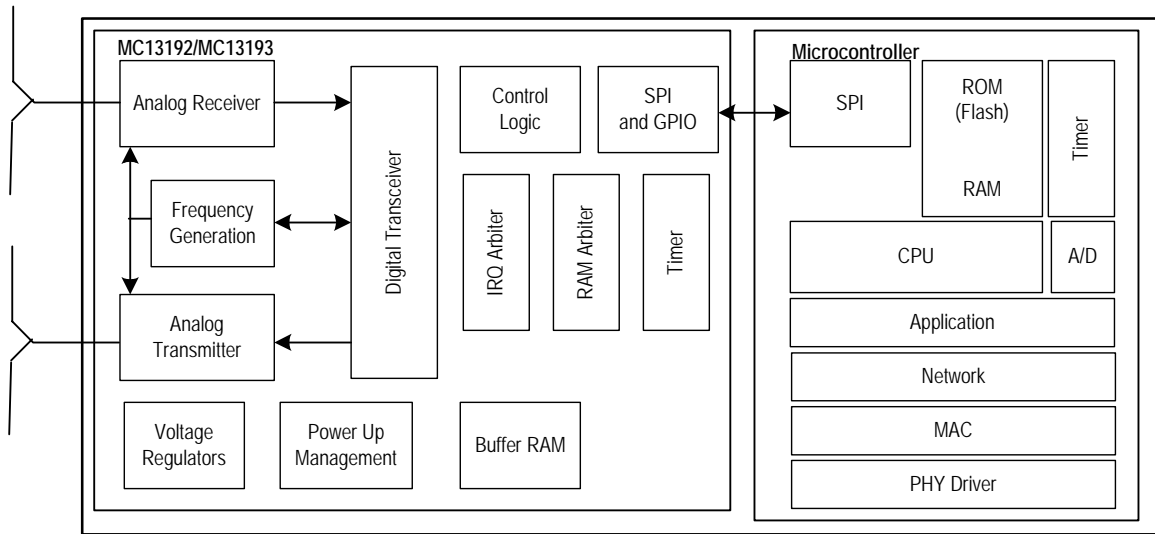


Figure 4. System Level Block Diagram

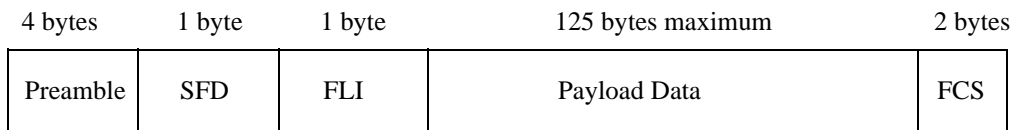


Figure 5. MC13192/MC13193 Packet Structure

## 5 Electrical Characteristics

### 5.1 Maximum Ratings

Table 1. Absolute Maximum Ratings

| Rating                    | Symbol                | Value      | Unit |
|---------------------------|-----------------------|------------|------|
| Power Supply Voltage      | $V_{BATT}, V_{DDINT}$ | 3.6        | Vdc  |
| RF Input Power            | $P_{max}$             | 10         | dBm  |
| Junction Temperature      | $T_J$                 | 125        | °C   |
| Storage Temperature Range | $T_{stg}$             | -55 to 125 | °C   |

**Note:** Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

**Note:** Meets Human Body Model (HBM) = 2 kV and Machine Model (MM) = 200 V except  $RFIN_{\pm} = 100$  V MM,  $PAO_{\pm} = 50$  V MM & 1 kV HBM, and  $VBATT = 100$  V MM. RF output pins have no ESD protection.

### 5.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

| Characteristic  | Symbol                | Min                | Typ | Max                | Unit |
|---|-----------------------|--------------------|-----|--------------------|------|
| Power Supply Voltage ( $V_{BATT} = V_{DDINT}$ )   | $V_{BATT}, V_{DDINT}$ | 2.0                | 2.7 | 3.4                | Vdc  |
| Input Frequency   | $f_{in}$              | 2.405              | -   | 2.480              | GHz  |
| Ambient Temperature Range   | $T_A$                 | -40                | 25  | 85                 | °C   |
| Logic Input Voltage Low   | $V_{IL}$              | 0                  | -   | 30%<br>$V_{DDINT}$ | V    |
| Logic Input Voltage High  | $V_{IH}$              | 70%<br>$V_{DDINT}$ | -   | $V_{DDINT}$        | V    |
| SPI Clock Rate  | $f_{SPI}$             | -                  | -   | 8.0                | MHz  |
| RF Input Power  | $P_{max}$             | -                  | -   | 10                 | dBm  |
| Crystal Reference Oscillator Frequency ( $\pm 40$ ppm over operating conditions to meet the 802.15.4 standard.) | $f_{ref}$             | 16 MHz Only        |     |                    |      |



## 5.3 DC Electrical Characteristics

**Table 3. DC Electrical Characteristics**

( $V_{BATT}$ ,  $V_{DDINT} = 2.7$  V,  $T_A = 25$  °C, unless otherwise noted)

| Characteristic   | Symbol        | Min                | Typ | Max                | Unit    |
|--|---------------|--------------------|-----|--------------------|---------|
| Power Supply Current ( $V_{BATT} + V_{DDINT}$ )                      |               |                    |     |                    |         |
| Off  | $I_{leakage}$ | -                  | 0.2 | 1.0                | $\mu$ A |
| Hibernate  | $I_{CCH}$     | -                  | 1.0 | 6.0                | $\mu$ A |
| Doze (No CLK0)   | $I_{CCD}$     | -                  | 35  | 102                | $\mu$ A |
| Idle   | $I_{CCI}$     | -                  | 500 | 800                | $\mu$ A |
| Transmit Mode (0 dBm nominal output power)                           | $I_{CCT}$     | -                  | 30  | 35                 | mA      |
| Receive Mode   | $I_{CCR}$     | -                  | 37  | 42                 | mA      |
| Input Current ( $V_{IN} = 0$ V or $V_{DDINT}$ ) (All digital inputs) | $I_{IN}$      | -                  | -   | $\pm 1$            | $\mu$ A |
| Input Low Voltage (All digital inputs)                               | $V_{IL}$      | 0                  | -   | 30%<br>$V_{DDINT}$ | V       |
| Input High Voltage (all digital inputs)                              | $V_{IH}$      | 70%<br>$V_{DDINT}$ | -   | $V_{DDINT}$        | V       |
| Output High Voltage ( $I_{OH} = -1$ mA) (All digital outputs)        | $V_{OH}$      | 80%<br>$V_{DDINT}$ | -   | $V_{DDINT}$        | V       |
| Output Low Voltage ( $I_{OL} = 1$ mA) (All digital outputs)          | $V_{OL}$      | 0                  | -   | 20%<br>$V_{DDINT}$ | V       |

## 5.4 AC Electrical Characteristics

### NOTE

All AC parameters measured with SPI Registers at default settings except where noted and the following registers over-programmed:

Register 08 = 0xFFF7 and Register 11 = 0x20FF

**Table 4. Receiver AC Electrical Characteristics**

( $V_{BATT}$ ,  $V_{DDINT}$  = 2.7 V,  $T_A$  = 25 °C,  $f_{ref}$  = 16 MHz, unless otherwise noted.)

Parameters measured at connector J6 of evaluation circuit.)

| Characteristic   | Symbol       | Min | Typ | Max | Unit |
|--|--------------|-----|-----|-----|------|
| Sensitivity for 1% Packet Error Rate (PER) (-40 to +85 °C) | $SENS_{per}$ | -   | -92 | -   | dBm  |
| Sensitivity for 1% Packet Error Rate (PER) (+25 °C)        |              | -   | -92 | -87 | dBm  |
| Saturation (maximum input level)                           | $SENS_{max}$ | -   | 10  | -   | dBm  |
| Channel Rejection for 1% PER (desired signal -82 dBm)      |              |     |     |     |      |
| +5 MHz (adjacent channel)                                  |              | -   | 25  | -   | dB   |
| -5 MHz (adjacent channel)                                  |              | -   | 31  | -   | dB   |
| +10 MHz (alternate channel)                                |              | -   | 42  | -   | dB   |
| -10 MHz (alternate channel)                                |              | -   | 41  | -   | dB   |
| >= 15 MHz  |              | -   | 49  | -   | dB   |
| Frequency Error Tolerance                                  |              | -   | -   | 200 | kHz  |
| Symbol Rate Error Tolerance                                |              | -   | -   | 80  | ppm  |

**Table 5. Transmitter AC Electrical Characteristics**

( $V_{BATT}$ ,  $V_{DDINT}$  = 2.7 V,  $T_A$  = 25 °C,  $f_{ref}$  = 16 MHz, unless otherwise noted.)

Parameters measured at connector J5 of evaluation circuit.)

| Characteristic   | Symbol    | Min | Typ | Max | Unit |
|--|-----------|-----|-----|-----|------|
| Power Spectral Density (-40 to +85 °C) Absolute limit  |           | -   | -47 | -   | dBm  |
| Power Spectral Density (-40 to +85 °C) Relative limit  |           | -   | 47  | -   |      |
| Nominal Output Power <sup>1</sup>                      | $P_{out}$ | -3  | 0   | 3   | dBm  |
| Maximum Output Power <sup>2</sup>                      |           |     | 4   |     | dBm  |
| Error Vector Magnitude                                 | EVM       | -   | 20  | 35  | %    |
| Output Power Control Range (-27 dBm to +4 dBm typical) |           | -   | 31  | -   | dB   |
| Over the Air Data Rate                                 |           | -   | 250 | -   | kbps |
| 2nd Harmonic   |           | -   | -42 | -   | dBc  |
| 3rd Harmonic   |           | -   | -44 | -   | dBc  |

<sup>1</sup> SPI Register 12 programmed to 0x00BC which sets output power to nominal (0 dBm typical).

<sup>2</sup> SPI Register 12 programmed to 0x00FC which sets output power to maximum.

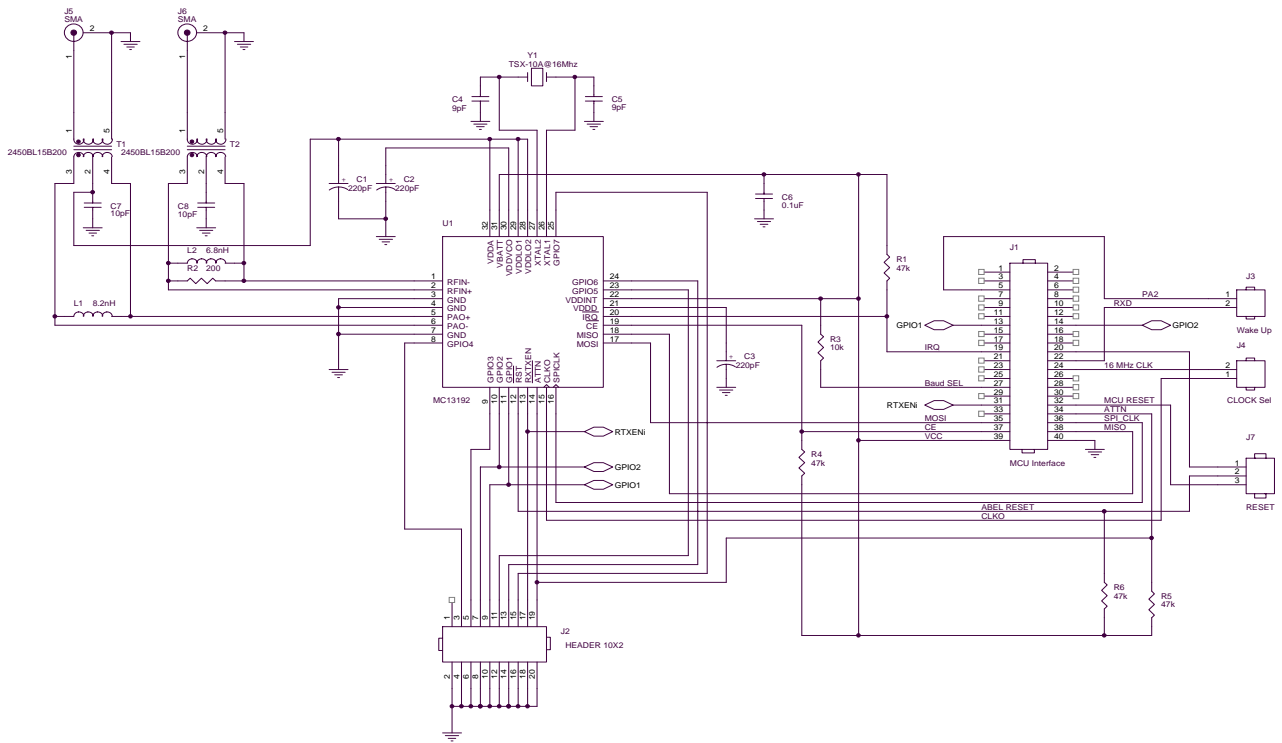


Figure 6. Parameter Evaluation Circuit

## 6 Functional Description

### 6.1 MC13192/MC13193 Operational Modes

The MC13192/MC13193 has a number of operational modes that allow for low-current operation. Transition from the Off to Idle mode occurs when  $\overline{\text{RST}}$  is negated. Once in Idle, the SPI is active and is used to control the IC. Transition to Hibernate and Doze modes is enabled via the SPI. These modes are summarized, along with the transition times, in Table 6. Current drain in the various modes is listed in Table 3, DC Electrical Characteristics.

**Table 6. MC13192/MC13193 Mode Definitions and Transition Times**

| Mode      | Definition  | Transition Time To or From Idle             |
|-----------|---|---|
| Off       | All IC functions Off, Leakage only. $\overline{\text{RST}}$ asserted. Digital outputs are tri-stated including $\overline{\text{IRQ}}$  | 25 ms to Idle                               |
| Hibernate | Crystal Reference Oscillator Off. (SPI not functional.) IC Responds to $\overline{\text{ATTN}}$ . Data is retained.   | 20 ms to Idle                               |
| Doze      | Crystal Reference Oscillator On but CLKO output available only if Register 7, Bit 9 = 1 for frequencies of 1 MHz or less. (SPI not functional.) Responds to $\overline{\text{ATTN}}$ and can be programmed to enter Idle Mode through an internal timer comparator. | $(300 + 1/\text{CLKO}) \mu\text{s}$ to Idle |
| Idle      | Crystal Reference Oscillator On with CLKO output available. SPI active.   |   |
| Receive   | Crystal Reference Oscillator On. Receiver On.   | 144 $\mu\text{s}$ from Idle                 |
| Transmit  | Crystal Reference Oscillator On. Transmitter On.  | 144 $\mu\text{s}$ from Idle                 |

### 6.2 Serial Peripheral Interface (SPI)

The host microcontroller directs the MC13192/MC13193, checks its status, and reads/writes data to the device through the 4-wire SPI port. The transceiver operates as a SPI slave device only. A transaction between the host and the MC13192/MC13193 occurs as multiple 8-bit bursts on the SPI. The SPI signals are:

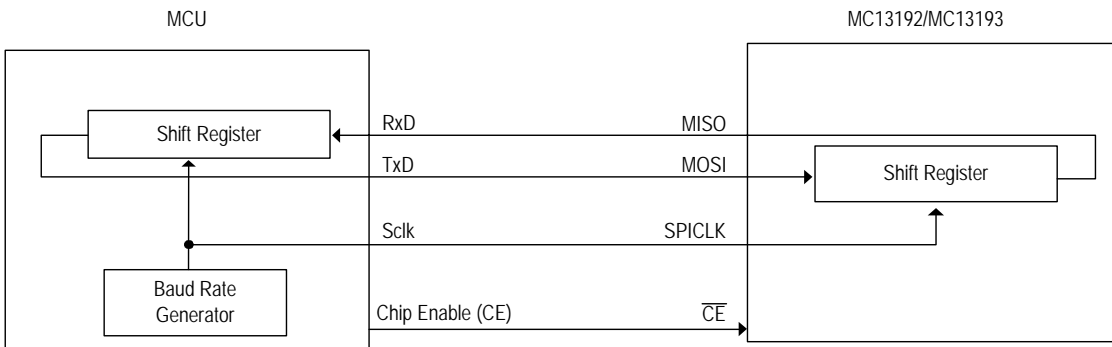
1. Chip Enable ( $\overline{\text{CE}}$ ) - A transaction on the SPI port is framed by the active low  $\overline{\text{CE}}$  input signal. A transaction is a minimum of 3 SPI bursts and can extend to a greater number of bursts.
2. SPI Clock (SPICLK) - The host drives the SPICLK input to the MC13192/MC13193. Data is clocked into the master or slave on the leading (rising) edge of the return-to-zero SPICLK and data out changes state on the trailing (falling) edge of SPICLK.

#### NOTE

For Freescale microcontrollers, the SPI clock format is the clock phase control bit  $\text{CPHA} = 0$  and the clock polarity control bit  $\text{CPOL} = 0$ .

3. Master Out/Slave In (MOSI) - Incoming data from the host is presented on the MOSI input.
4. Master In/Slave Out (MISO) - The MC13192/MC13193 presents data to the master on the MISO output.

A typical interconnection to a microcontroller is shown in [Figure 7](#).

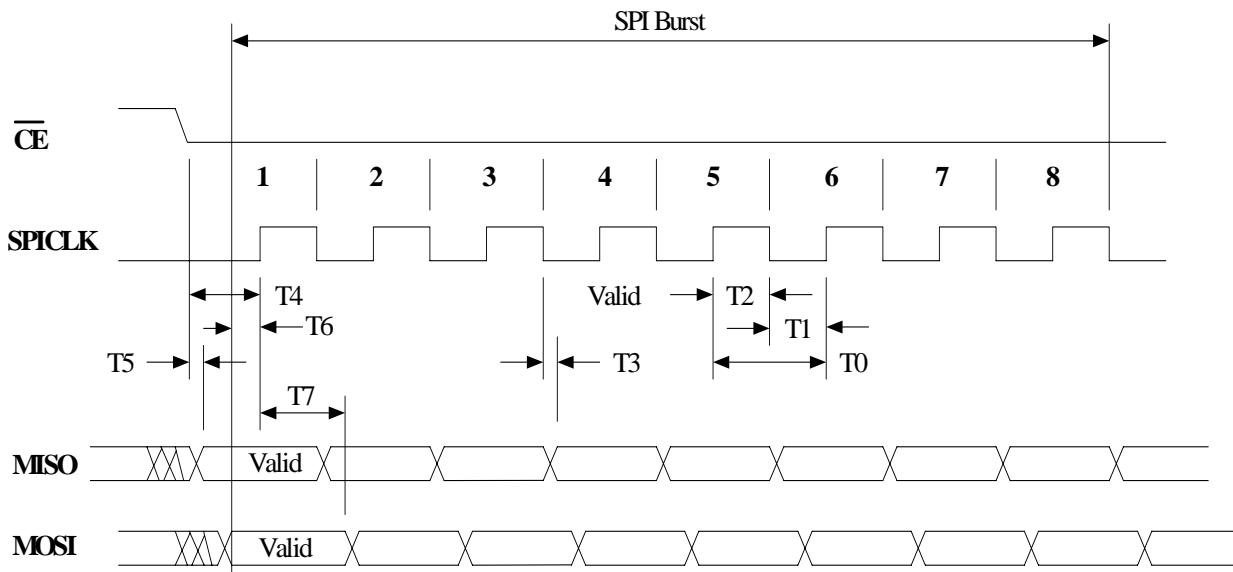


**Figure 7. SPI Interface**

Although the SPI port is fully static, internal memory, timer and interrupt arbiters require an internal clock ( $CLK_{core}$ ), derived from the crystal reference oscillator, to communicate from the SPI registers to internal registers and memory.

### 6.2.1 SPI Burst Operation

The SPI port of an MCU transfers data in bursts of 8 bits with most significant bit (MSB) first. The master (MCU) can send a byte to the slave (transceiver) on the MOSI line and the slave can send a byte to the master on the MISO line. Although an MC13192/MC13193 transaction is three or more SPI bursts long, the timing of a single SPI burst is shown in [Figure 8](#).



**Figure 8. SPI Single Burst Timing Diagram**

Table 7. SPI Timing Specifications

| Symbol | Parameter  | Min  | Typ | Max | Unit |
|--------|--|------|-----|-----|------|
| T0     | SPICLK period                                    | 125  |     |     | nS   |
| T1     | Pulse width, SPICLK low                          | 62.5 |     |     | nS   |
| T2     | Pulse width, SPICLK high                         | 62.5 |     |     | nS   |
| T3     | Delay time, MISO data valid from falling SPICLK  |      | 15  |     | nS   |
| T4     | Setup time, $\overline{CE}$ low to rising SPICLK |      | 15  |     | nS   |
| T5     | Delay time, MISO valid from $\overline{CE}$ low  |      | 15  |     | nS   |
| T6     | Setup time, MOSI valid to rising SPICLK          |      | 15  |     | nS   |
| T7     | Hold time, MOSI valid from rising SPICLK         |      | 15  |     | nS   |

## 6.2.2 SPI Transaction Operation

Although the SPI port of an MCU transfers data in bursts of 8 bits, the MC13192/MC13193 requires that a complete SPI transaction be framed by  $\overline{CE}$ , and there will be three (3) or more bursts per transaction. The assertion of  $\overline{CE}$  to low signals the start of a transaction. The first SPI burst is a write of an 8-bit header to the transceiver (MOSI is valid) that defines a 6-bit address of the internal resource being accessed and identifies the access as being a read or write operation. In this context, a write is data written to the MC13192/MC13193 and a read is data written to the SPI master. The following SPI bursts will be either the write data (MOSI is valid) to the transceiver or read data from the transceiver (MISO is valid).

Although the SPI bus is capable of sending data simultaneously between master and slave, the MC13192/MC13193 never uses this mode. The number of data bytes (payload) will be a minimum of 2 bytes and can extend to a larger number depending on the type of access. After the final SPI burst,  $\overline{CE}$  is negated to high to signal the end of the transaction. Refer to the *MC13192/MC13193 Reference Manual*, part number MC13192RM for more details on SPI registers and transaction types.

An example SPI read transaction with a 2-byte payload is shown in [Figure 9](#).

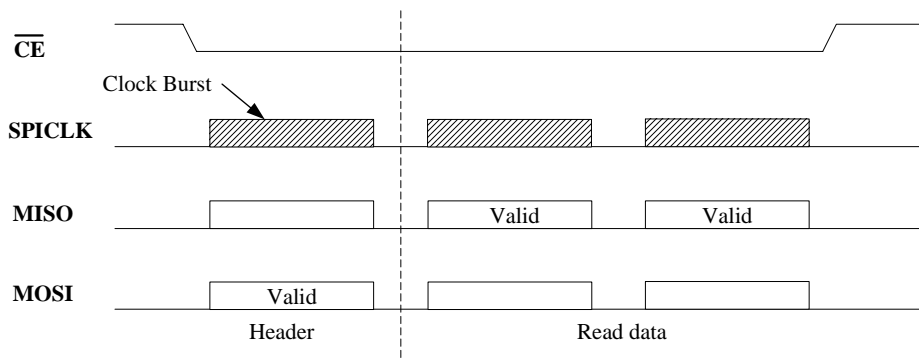


Figure 9. SPI Read Transaction Diagram

## 7 Pin Connections

Table 8. Pin Function Description

| Pin # | Pin Name                 | Type                  | Description  | Functionality                      |
|-------|--------------------------|-----------------------|--|------------------------------------|
| 1     | RFIN-                    | RF Input              | LNA negative differential input.   |                                    |
| 2     | RFIN+                    | RF Input              | LNA positive differential input.   |                                    |
| 3     | Not Used                 |                       | Tie to Ground.   |                                    |
| 4     | Not Used                 |                       | Tie to Ground.   |                                    |
| 5     | PAO+                     | RF Output /DC Input   | Power Amplifier Positive Output. Open drain. Connect to $V_{DDA}$ .  |                                    |
| 6     | PAO-                     | RF Output/DC Input    | Power Amplifier Negative Output. Open drain. Connect to $V_{DDA}$ .  |                                    |
| 7     | SM                       |                       | Test mode pin. Tie to Ground   | Tie to Ground for normal operation |
| 8     | GPIO4 <sup>1</sup>       | Digital Input/ Output | General Purpose Input/Output 4.  | See Footnote 1                     |
| 9     | GPIO3 <sup>1</sup>       | Digital Input/ Output | General Purpose Input/Output 3.  | See Footnote 1                     |
| 10    | GPIO2 <sup>1</sup>       | Digital Input/ Output | General Purpose Input/Output 2. When <code>gpio_alt_en</code> , Register 9, Bit 7 = 1, GPIO2 functions as a "CRC Valid" indicator.   | See Footnote 1                     |
| 11    | GPIO1 <sup>1</sup>       | Digital Input/ Output | General Purpose Input/Output 1. When <code>gpio_alt_en</code> , Register 9, Bit 7 = 1, GPIO1 functions as an "Out of Idle" indicator.  | See Footnote 1                     |
| 12    | $\overline{\text{RST}}$  | Digital Input         | Active Low Reset. While held low, the IC is in Off Mode and all internal information is lost from RAM and SPI registers. When high, IC goes to IDLE Mode, with SPI in default state.   |                                    |
| 13    | RXTXEN                   | Digital Input         | Active High. Low to high transition initiates RX or TX sequence depending on SPI setting. Should be taken high after SPI programming to start RX or TX sequence and should be held high through the sequence. After sequence is complete, return RXTXEN to low. When held low, forces Idle Mode. |                                    |
| 14    | $\overline{\text{ATTN}}$ | Digital Input         | Active Low Attention. Transitions IC from either Hibernate or Doze Modes to Idle.  |                                    |
| 15    | CLKO                     | Digital Output        | Clock output to host MCU. Programmable frequencies of:<br>16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 62.5 kHz, 32.786+ kHz (default), and 16.393+ kHz.  |                                    |
| 16    | SPICLK                   | Digital Clock Input   | External clock input for the SPI interface.  |                                    |

Table 8. Pin Function Description (continued)

| Pin # | Pin Name                | Type                 | Description   | Functionality   |
|-------|-------------------------|----------------------|---|---|
| 17    | MOSI                    | Digital Input        | Master Out/Slave In. Dedicated SPI data input.  |   |
| 18    | MISO                    | Digital Output       | Master In/Slave Out. Dedicated SPI data output.   |   |
| 19    | $\overline{\text{CE}}$  | Digital Input        | Active Low Chip Enable. Enables SPI transfers.  |   |
| 20    | $\overline{\text{IRQ}}$ | Digital Output       | Active Low Interrupt Request.   | Open drain device. Programmable 40 k $\Omega$ internal pull-up. Interrupt can be serviced every 6 $\mu\text{s}$ with <20 pF load. Optional external pull-up must be >4 k $\Omega$ . |
| 21    | VDDD                    | Power Output         | Digital regulated supply bypass.  | Decouple to ground.   |
| 22    | VDDINT                  | Power Input          | Digital interface supply & digital regulator input. Connect to Battery.   | 2.0 to 3.4 V. Decouple to ground.   |
| 23    | GPIO5 <sup>1</sup>      | Digital Input/Output | General Purpose Input/Output 5.   | See Footnote 1  |
| 24    | GPIO6 <sup>1</sup>      | Digital Input/Output | General Purpose Input/Output 6.   | See Footnote 1  |
| 25    | GPIO7 <sup>1</sup>      | Digital Input/Output | General Purpose Input/Output 7.   | See Footnote 1  |
| 26    | XTAL1                   | Input                | Crystal Reference oscillator input.   | Connect to 16 MHz crystal and load capacitor.   |
| 27    | XTAL2                   | Input/Output         | Crystal Reference oscillator output<br><b>Note:</b> Do not load this pin by using it as a 16 MHz source. Measure 16 MHz output at Pin 15, CLK0, programmed for 16 MHz. See the <i>MC13192/MC13193 Reference Manual</i> for details. | Connect to 16 MHz crystal and load capacitor.   |
| 28    | VDDL02                  | Power Input          | LO2 VDD supply. Connect to VDDA externally.   |   |
| 29    | VDDL01                  | Power Input          | LO1 VDD supply. Connect to VDDA externally.   |   |
| 30    | VDDVCO                  | Power Output         | VCO regulated supply bypass.  | Decouple to ground.   |
| 31    | VBATT                   | Power Input          | Analog voltage regulators Input. Connect to Battery.  | Decouple to ground.   |
| 32    | VDDA                    | Power Output         | Analog regulated supply Output. Connect to directly VDDL01 and VDDL02 externally and to PAO $\pm$ through a frequency trap.<br><b>Note:</b> Do not use this pin to supply circuitry external to the chip.                           | Decouple to ground.   |
| EP    | Ground                  |                      | External paddle / flag ground.  | Connect to ground.  |

<sup>1</sup> The transceiver GPIO pins default to inputs at reset. There are no programmable pullups on these pins. Unused GPIO pins should be tied to ground if left as inputs, or if left unconnected, they should be programmed as outputs set to the low state.



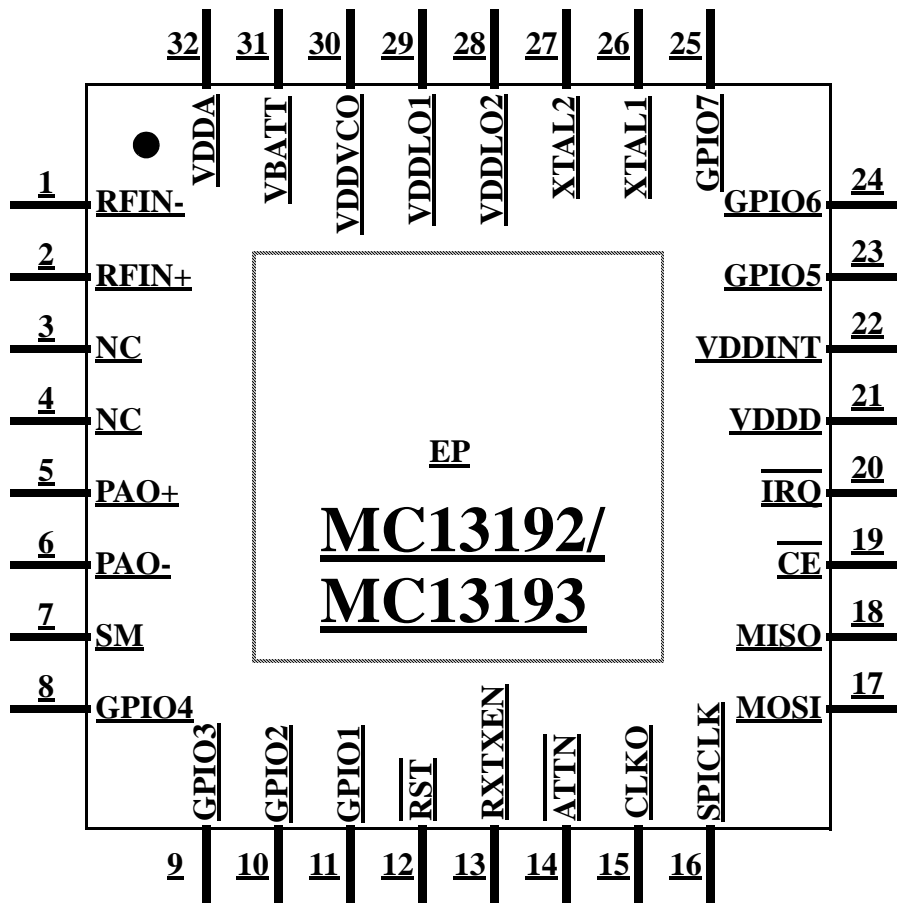


Figure 10. Pin Connections (Top View)

## 8 Applications Information

### 8.1 Crystal Oscillator Reference Frequency

The IEEE 802.15.4 Standard requires that several frequency tolerances be kept within  $\pm 40$  ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will still result in acceptable performance. The MC13192/MC13193 transceiver provides onboard crystal trim capacitors to assist in meeting this performance.

The primary determining factor in meeting this specification is the tolerance of the crystal oscillator reference frequency. A number of factors can contribute to this tolerance and a crystal specification will quantify each of them:

1. The initial (or make) tolerance of the crystal resonant frequency itself.
2. The variation of the crystal resonant frequency with temperature.
3. The variation of the crystal resonant frequency with time, also commonly known as aging.
4. The variation of the crystal resonant frequency with load capacitance, also commonly known as pulling. This is affected by:
  - a) The external load capacitor values - initial tolerance and variation with temperature.
  - b) The internal trim capacitor values - initial tolerance and variation with temperature.
  - c) Stray capacitance on the crystal pin nodes - including stray on-chip capacitance, stray package capacitance and stray board capacitance; and its initial tolerance and variation with temperature.

Freescall has specified that a 16 MHz crystal with a  $<9$  pF load capacitance is required. The MC13192/MC13193 does not contain a reference divider, so 16 MHz is the only frequency that can be used. A crystal requiring higher load capacitance is prohibited because a higher load on the amplifier circuit may compromise its performance. The crystal manufacturer defines the load capacitance as that total external capacitance seen across the two terminals of the crystal. The oscillator amplifier configuration used in the MC13192/MC13193 requires two balanced load capacitors from each terminal of the crystal to ground. As such, the capacitors are seen to be in series by the crystal, so each must be  $<18$  pF for proper loading.

In the reference schematic, the external load capacitors are shown as 6.8 pF each, used in conjunction with a crystal that requires an 8 pF load capacitance. The default internal trim capacitor value (2.4 pF) and stray capacitance total value (6.8 pF) sum up to 9.2 pF giving a total of 16 pF. The value for the stray capacitance was determined empirically assuming the default internal trim capacitor value and for a specific board layout. A different board layout may require a different external load capacitor value. The on-chip trim capability may be used to determine the closest standard value by adjusting the trim value via the SPI and observing the frequency at CLK0. Each internal trim load capacitor has a trim range of approximately 5 pF in 20 fF steps.

Initial tolerance for the internal trim capacitance is approximately  $\pm 15\%$ .

Since the MC13192/MC13193 contains an on-chip reference frequency trim capability, it is possible to trim out virtually all of the initial tolerance factors and put the frequency within 0.12 ppm on a board-by-board basis.

A tolerance analysis budget may be created using all the previously stated factors. It is an engineering judgment whether the worst case tolerance will assume that all factors will vary in the same direction or if the various factors can be statistically rationalized using RSS (Root-Sum-Square) analysis. The aging factor is usually specified in ppm/year and the product designer can determine how many years are to be assumed for the product lifetime. Taking all of the factors into account, the product designer can determine the needed specifications for the crystal and external load capacitors to meet the IEEE 802.15.4 specification.

## 8.2 Design Example

Figure 11 shows a basic application schematic for interfacing the MC13192/MC13193 with an MCU. Table 9 lists the Bill of Materials (BOM).

The MC13192/MC13193 has differential RF inputs and outputs that are well suited to balanced printed wire antenna structures. Alternatively, as in the application circuit, a printed wire antenna, a chip antenna, or other single-ended structures can be used with commercially available chip baluns or microstrip equivalents. PAO+ and PAO- require a DC connection to VDDA (the analog regulator output) through AC blocking elements. This is accomplished through the baluns in the referenced design.

The 16 MHz crystal should be mounted close to the MC13192/MC13193 because the crystal trim default assumes that the listed KDS Daishinku crystal (see Table 10) and the 6.8 pF load capacitors shown are used. If a different crystal is used, it should have a specified load capacitance (stray capacitance, etc.) of 9 pF or less. A second crystal that has been evaluated and also gives acceptable performance is the Toyocom TSX-10A 16 MHz TN4-26139 (see Table 11).

VDDA is an analog regulator output used to supply only the onboard PA (PAO+ and PAO-) and VDDLO1 and VDDLO2 pins. VDDA should not be used to power devices external to the transceiver chip. Bypassing capacitors are critical and should be placed close to the device. Unused pins should be grounded as shown.

The SPI connections to the MCU include  $\overline{CE}$ , MOSI, MISO, and SPICLK. The SPI can run at a frequency of 8 MHz or less. Optionally, CLKO can provide a clock to the MCU. The CLKO frequency is programmable via the SPI and has a default of 32.786+ kHz (16 MHz / 488). The  $\overline{ATTN}$  line can be driven by a GPIO from the MCU (as shown) or can also be controlled by a switch or other hardware. The latter approach allows the MCU to be put into a sleep mode and then awakened by CLKO when the  $\overline{ATTN}$  line wakes up the MC13192/MC13193. RXTXEN is used to initiate receive, transmit or CCA/ED sequences under MCU control. RXTXEN must be controlled by an MCU GPIO with the connection shown. Device reset ( $\overline{RST}$ ) is controlled through a connection to an MCU GPIO.

When the MC13192/MC13193 is used in Stream Mode, as with 802.15.4 MAC/PHY software, the MC13192/MC13193 GPIO1 functions as an “Out of Idle” indicator and GPIO2 functions as a “CRC Valid” / Clear Channel Assessment (CCA) result indicator and are not available for general purpose use.

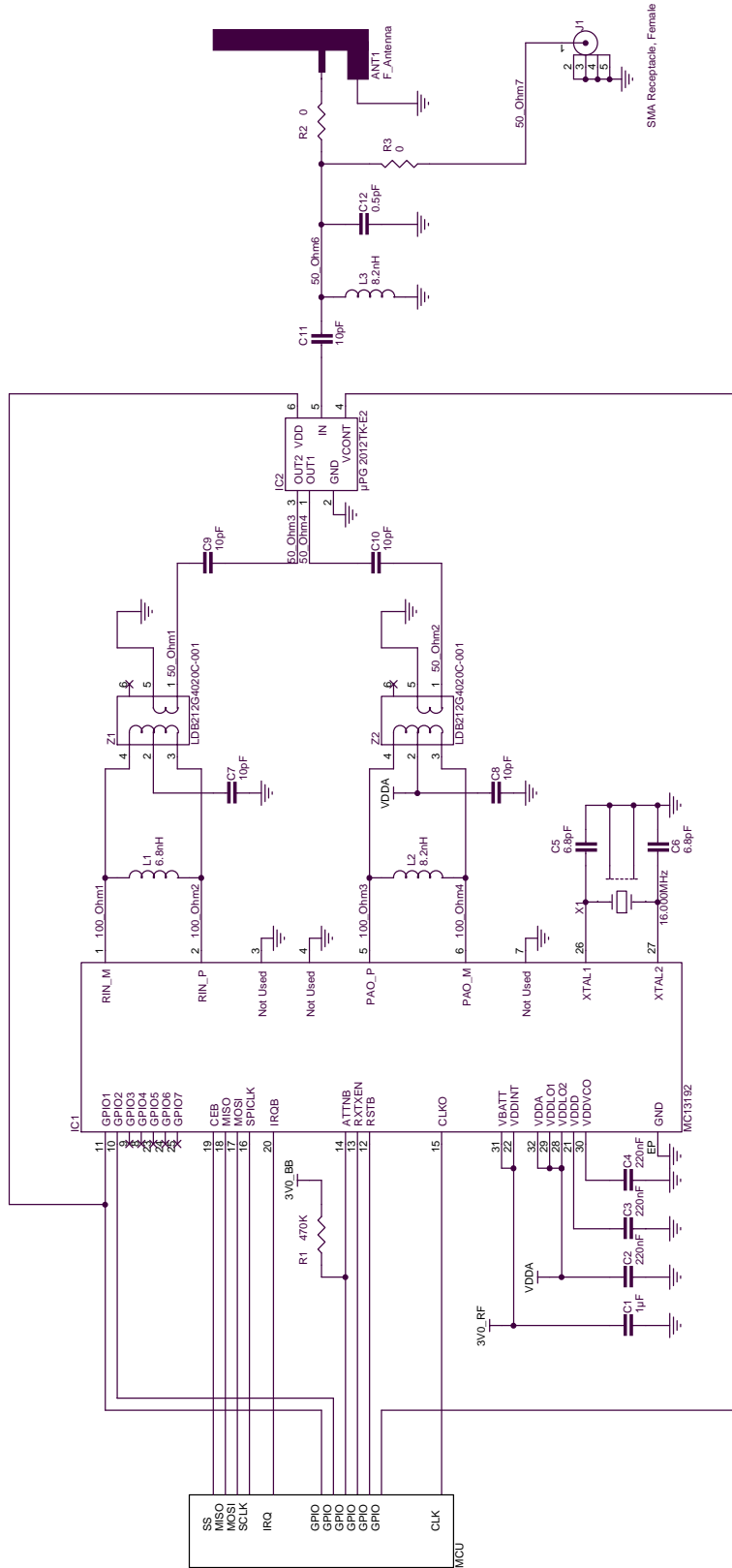


Figure 11. MC13192/MC13193 Configured With a MCU

Table 9. MC13192/MC13193 to MCU Bill of Materials (BOM)

| Item | Quantity | Reference            | Part                              | Manufacturer            |
|------|----------|----------------------|-----------------------------------|-------------------------|
| 1    | 1        | ANT1                 | F_Antenna                         | Printed wire            |
| 2    | 1        | C1                   | 1 $\mu$ F                         |                         |
| 3    | 3        | C2, C3, C4           | 220 nF                            |                         |
| 4    | 2        | C5, C6               | 6.8 pF                            |                         |
| 5    | 5        | C7, C8, C9, C10, C11 | 10 pF                             |                         |
| 6    | 1        | C12                  | 0.5 pF                            |                         |
| 7    | 1        | IC1                  | MC13192/MC13193                   | Freescale Semiconductor |
| 8    | 1        | IC2                  | $\mu$ PG2012TK-E2                 | NEC                     |
| 9    | 1        | J1                   | SMA Receptacle, Female            |                         |
| 10   | 1        | L1                   | 6.8 nH                            |                         |
| 11   | 2        | L2, L3               | 8.2 nH                            |                         |
| 12   | 1        | R1                   | 470 k $\Omega$                    |                         |
| 13   | 2        | R2, R3               | 0 $\Omega$                        |                         |
| 14   | 1        | X1                   | 16.000 MHz, Type DSX321G, ZD00882 | KDS, Daishinku Corp     |
| 15   | 2        | Z1, Z2               | LDB212G4020C-001                  | Murata                  |

Table 10. Daishinku KDS - DSX321G ZD00882 Crystal Specifications

| Parameter                    | Value    | Unit     | Condition                               |
|------------------------------|----------|----------|---|
| Type                         | DSX321G  |          | surface mount                           |
| Frequency                    | 16       | MHz      |   |
| Frequency tolerance          | $\pm 20$ | ppm      | at 25 $^{\circ}$ C $\pm 3$ $^{\circ}$ C |
| Equivalent series resistance | 100      | $\Omega$ | max                                     |
| Temperature drift            | $\pm 20$ | ppm      | -10 $^{\circ}$ C to +60 $^{\circ}$ C    |
| Load capacitance             | 8.0      | pF       |   |
| Drive level                  | 10       | $\mu$ W  | $\pm 2$ $\mu$ W                         |
| Shunt capacitance            | 2        | pF       | max                                     |
| Mode of oscillation          |          |          | fundamental                             |

**Table 11. Toyocom TSX-10A 16MHZ TN4-26139 Crystal Specifications**

| Parameter                    | Value   | Unit | Condition        |
|------------------------------|---------|------|------------------|
| Type                         | TSX-10A |      | surface mount    |
| Frequency                    | 16      | MHz  |                  |
| Frequency tolerance          | ± 10    | ppm  | at 25 °C ± 3 °C  |
| Equivalent series resistance | 40      | Ω    | max              |
| Temperature drift            | ± 16    | ppm  | -40 °C to +85 °C |
| Load capacitance             | 9       | pF   |                  |
| Drive level                  | 100     | μW   | max              |
| Shunt capacitance            | 1.2     | pF   | typical          |
| Mode of oscillation          |         |      | fundamental      |



**How to Reach Us:**

**Home Page:**  
[www.freescale.com](http://www.freescale.com)

**E-mail:**  
[support@freescale.com](mailto:support@freescale.com)

**USA/Europe or Locations Not Listed:**  
Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
+1-800-521-6274 or +1-480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

**Europe, Middle East, and Africa:**  
Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

**Japan:**  
Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064, Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

**Asia/Pacific:**  
Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

**For Literature Requests Only:**  
Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-521-6274 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2004, 2005. All rights reserved.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.